A SPACE-RATED SOFT IP-CORE COMPATIBLE WITH THE PIC® HARDWARE ARCHITECTURE AND INSTRUCTION SET

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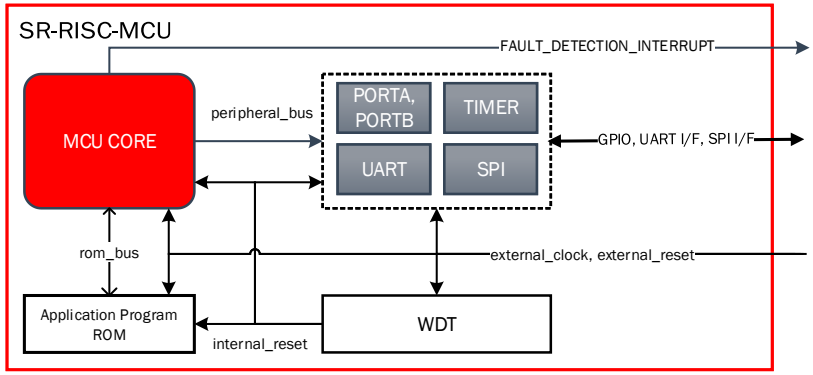
SAPIENZA
UNIVERSITÀ DI ROMA

Heritage

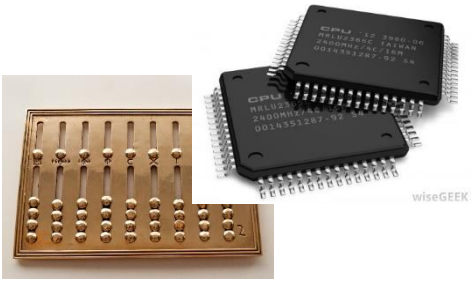
- This work inherits from a master degree thesis topic originated by:
  - ing. Davide Fiorini, Leonardo SpA
  - ing. Fabrizio Bernardini, FBIS
- and developed with the assistance and support of:
  - Leonardo SpA – Sistemi Avionici e Spaziali
  - The British Interplanetary Society

Presentation outline

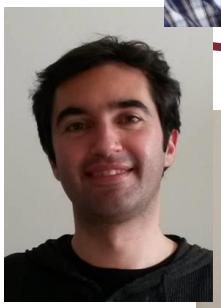
- Who we are
- Space environment effects on integrated circuits
- The ESA/ECSS FPGA/ASIC development cycle
- MCU soft-core design
- MCU soft-core hardware validation
- Conclusions and future perspectives



Digital System Lab group at Sapienza University

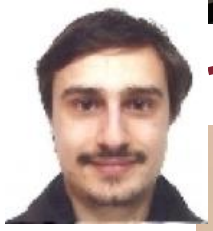


Mauro Olivieri, PhD, Associate Professor



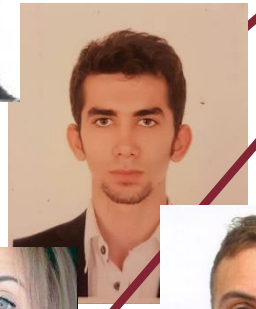
Francesco Menichelli, PhD, Assistant Professor

Antonio Mastrandrea, PhD, Research Fellow



Francesco Lannutti, PhD, Freelance Collaborator

Abdallah Cheikh, PhD candidate

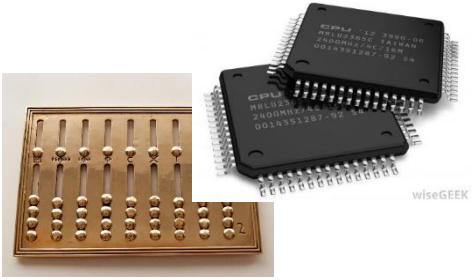


Giulia Stazi, PhD candidate

Luigi Blasi, PhD candidate & designer at ELT Spa

- **… +** on average, 3 Master Thesis candidates active in the group

Areas of activity and competences



- **Advanced embedded HW/SW development**
  - Linux, Embedded Linux, kernel programming, driver development
  - ARM, PIC, STM32 embedded system HW/SW development
  - Zigbee-compatible wireless-sensor-networks
- **Architecture modeling/evaluation** (single- & multi-core)
  - ARM, Leon, ST200, domain-specific (e.g. fuzzy, DSP)
  - Modeling languages: Qemu, SystemC, C, VHDL
- **RTL semi-custom IP design**
  - arithmetic units, codecs, JPEG2000 compression, neural architectures
  - FPGA and ASIC flow (primarily VHDL based)
- **Circuit design**
  - CMOS cell design, timing, power, reliability analysis (SPICE level)
  - Self-timing, delay insensitive logic, globally-asynch-locally-synch. logic

(Milano, Catania)

United Technologies
(ALES – Roma)

(Avezzano, Catania)

(Eindhoven- NL)

Univ. of Bologna

(Roma)

Univ. of Genoa

Polit. of Torino

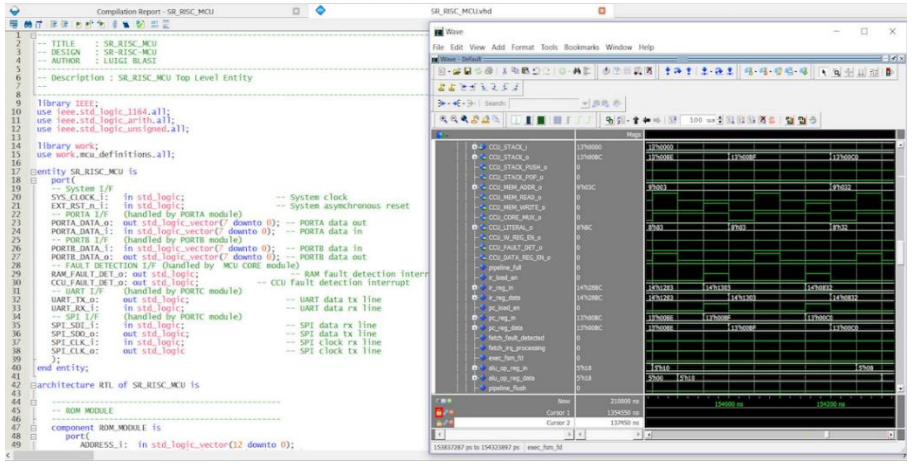
(Roma, Firenze)

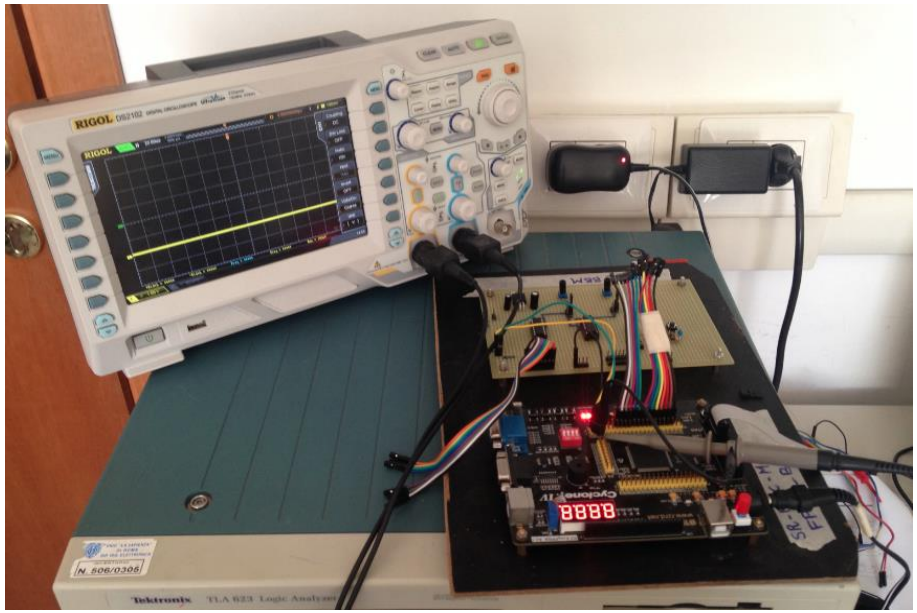
(Roma)

Project at a glance

Space-rated soft IP-core, synthesizable on FPGAs

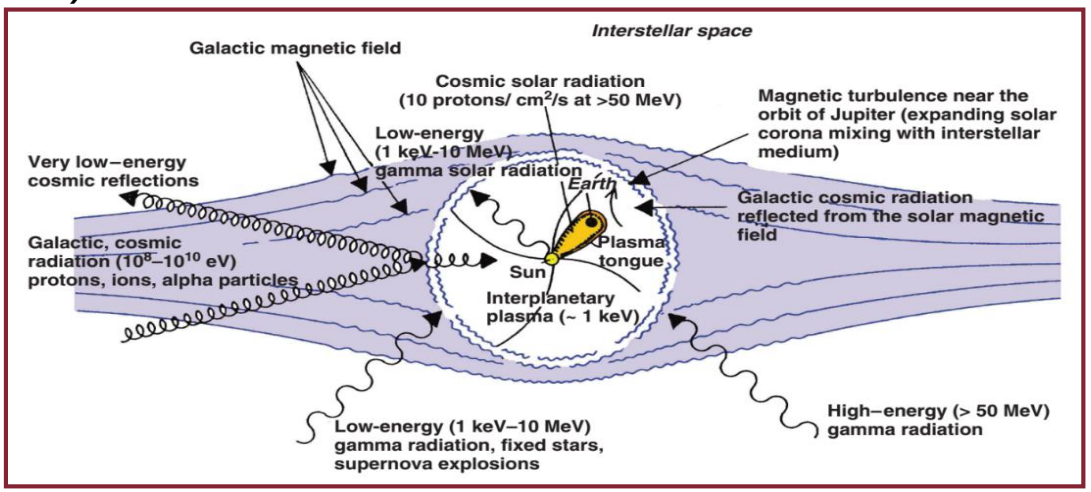
- Compliant with ECSS-Q-ST-60-02-C ESA standard industrial design cycle recommendations
- Compatible with:
  - Microchip® Midrange MCU hardware architecture
  - Microchip® Midrange MCU Instruction Set architecture
- Designed to operate in space environmental conditions
- Validated according to ESA/ECSS standards





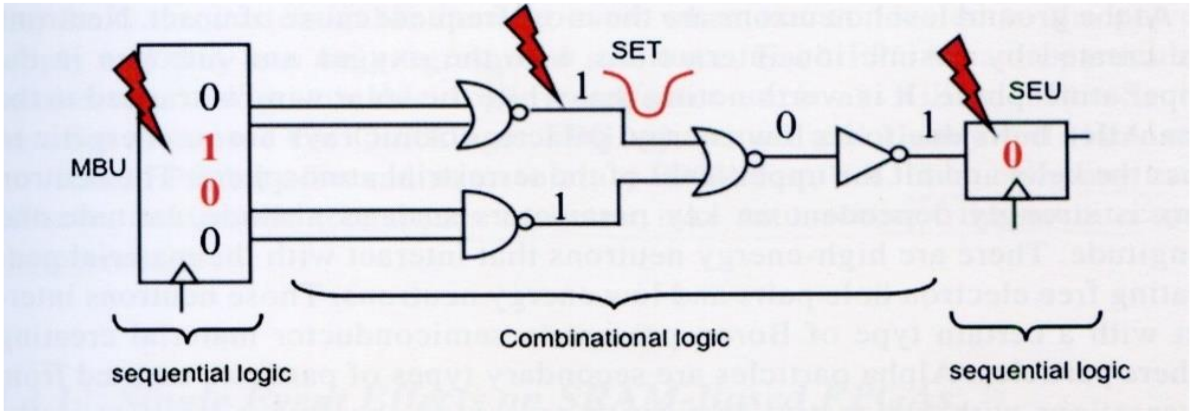
The radiation environment

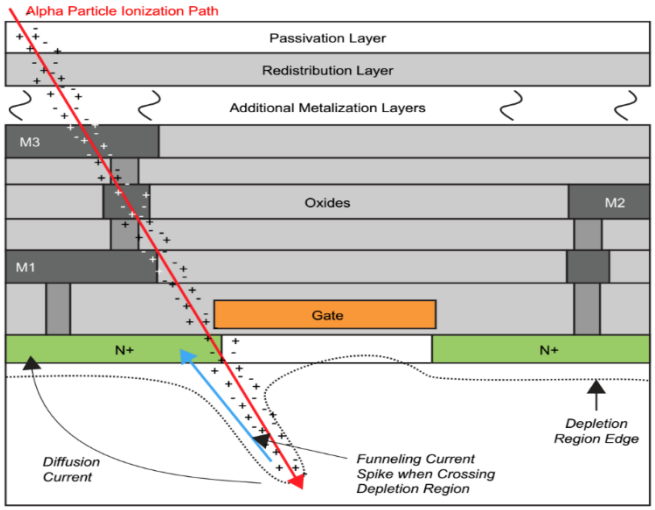
- The space environment presents various high-energy particles that can induce several effects on spacecraft electronics.
  - For this reason special qualification is required for every component used in space-related designs.
- Particles classification:
  - Energetic particles (electrons, protons and heavy ions)
  - Electromagnetic radiation (photons)
  - Uncharged particles (neutrons)
- Particles sources:
  - Van Allen Belts (trapped)
  - Magnetosphere (trapped)
  - Galactic Cosmic Rays
  - Solar Particles Events



Radiation effects on digital integrated circuits

- Cumulative Effects (TID and DD)
  - Long-term changes in devices characteristics (parametric degradation and functional failure)
- Single Event Effects (SEE)
  - Direct ionization (heavy ions/low energy protons) and secondary ionization (high energy protons)
    - Transient (SEU,SET,MBU,SEFI)
    - Permanent (SEL,SESB,SEGR,SEHE)

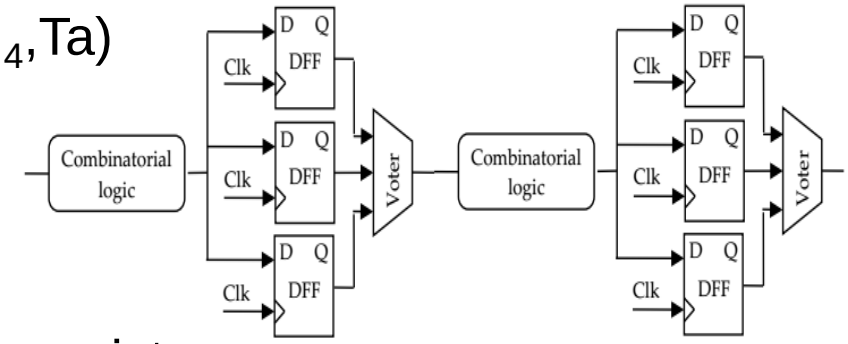




Alpha Particle: Helium Nucleus (2 Neutrons & 2 Protons)
Need a Charged Particle to Cause Ionization

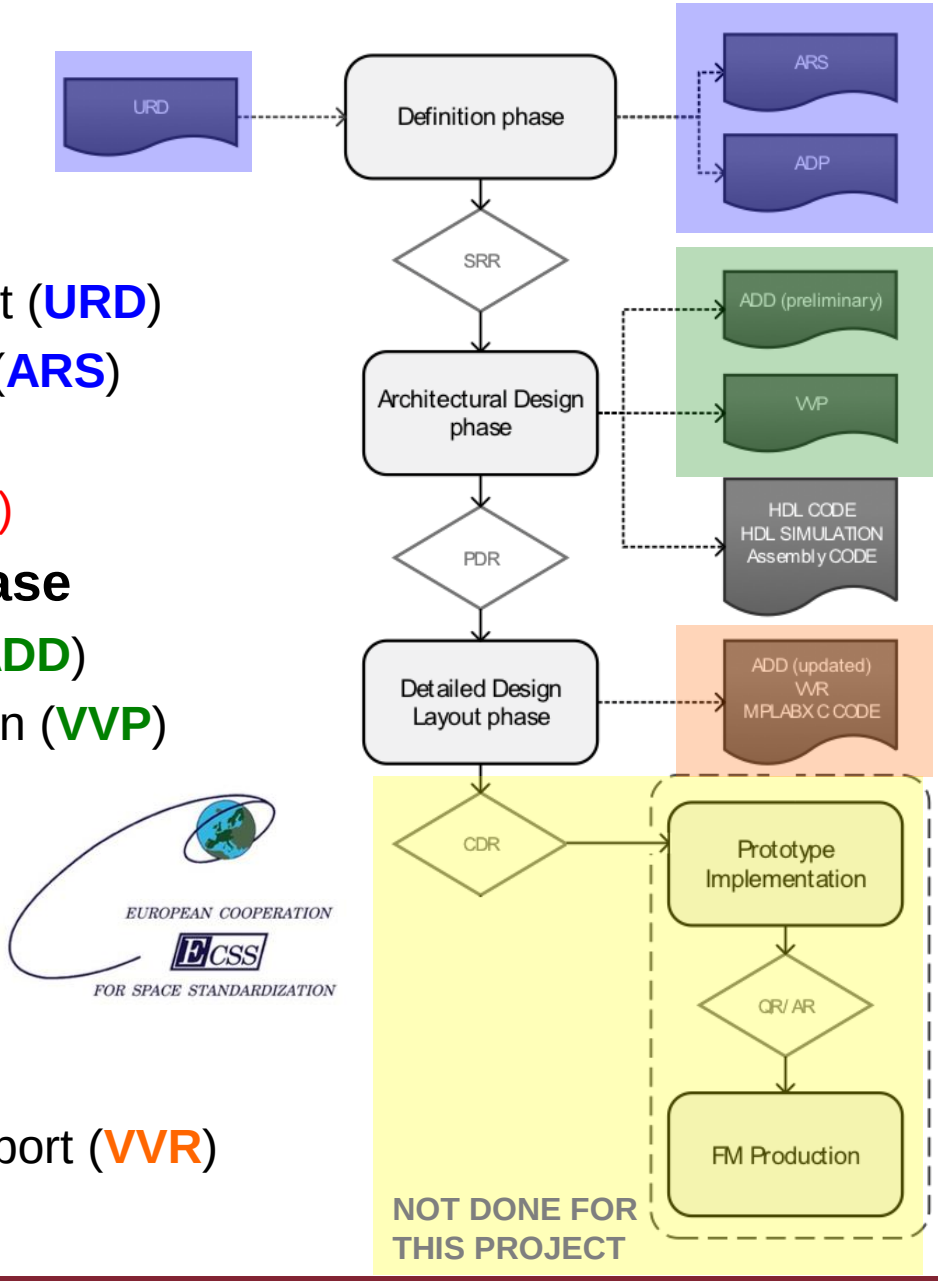
Design-level radiation mitigation techniques

- Total Ionizing Dose (TID) and Displacement Damage (DD)
  - Heavy or Light Shielding (Al,W,C_2H_4,Ta)
- Single Event Effects (SEEs)
  - Usage of rad-hard devices
  - Spatial Redundancy (local-TMR) for registers
  - Information Redundancy (SEC-DED) for SRAM cells
  - Memory block protection (Bit Interleaving) for SRAM cells
  - Instruction Execution Flow control (Watch-dog Timer)
  - Power Cycling and/or Hard Reset



The ECSS design flow

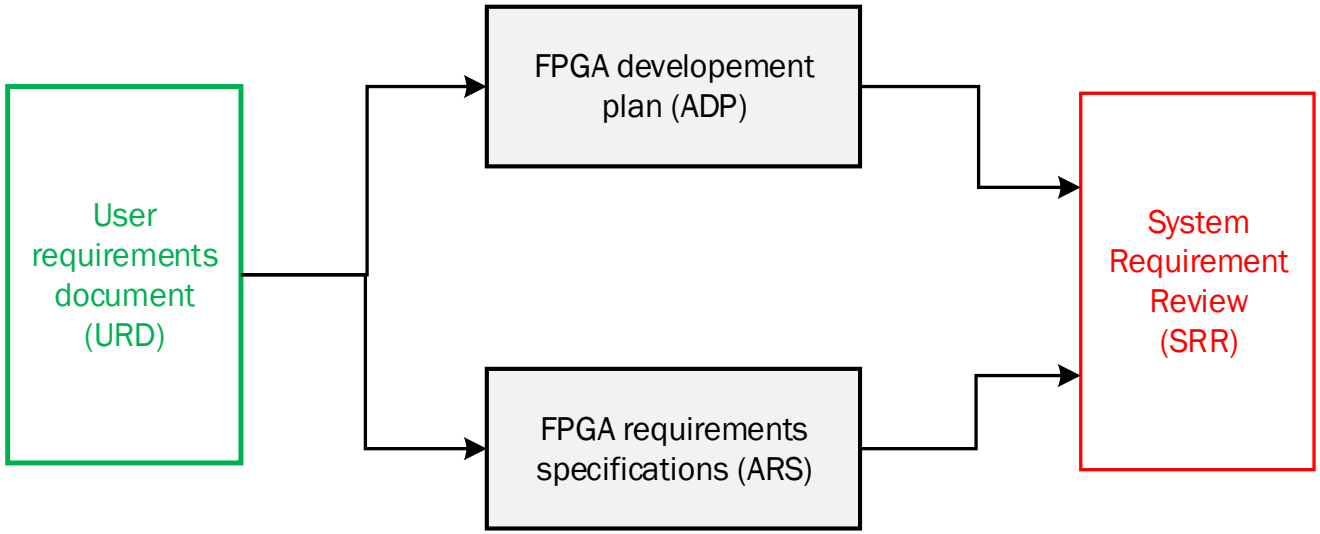
- **Phase 1: Definition Phase**
  - FPGA User Requirements Document (**URD**)
  - FPGA Requirements Specifications (**ARS**)
  - FPGA Developement Plan (**ADP**)
  - System Requirements Review (SSR)
- **Phase 2: Architectural Design Phase**
  - FPGA Detailed Design Document (**ADD**)
  - FPGA Verification and Validation Plan (**VVP**)
  - Preliminary Design Review (PDR)
- **Phase 3: Detailed Design Phase**
  - FPGA synthesis
  - FPGA_BBM validation test
    - With TEST Breadboard Model
  - FPGA Verification and Validation Report (**VVR**)
  - Critical Design Review (CDR)



EUROPEAN COOPERATION ECSS FOR SPACE STANDARDIZATION

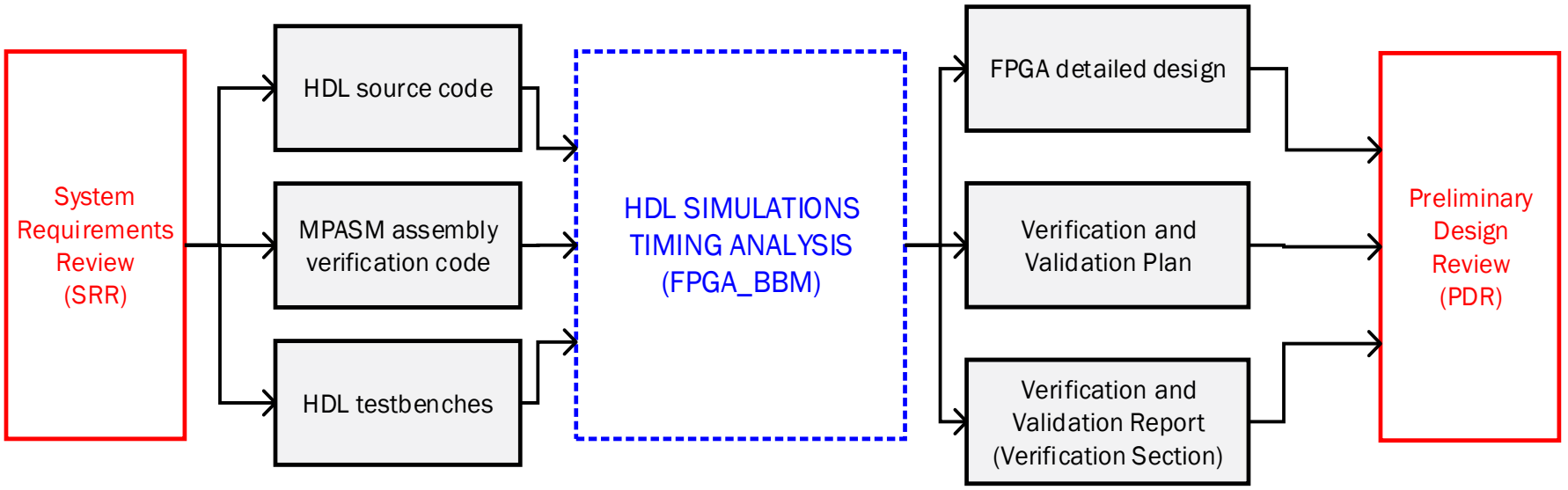
Definition Phase

- Definition of top-level requirements **FPGA User Requirements Document (URD)**
- Analysis of the PICmicro (COTS) MCU
- Production of the **FPGA Requirements Specifications (ARS)**
- Production of the **FPGA Development Plan (ADP)**



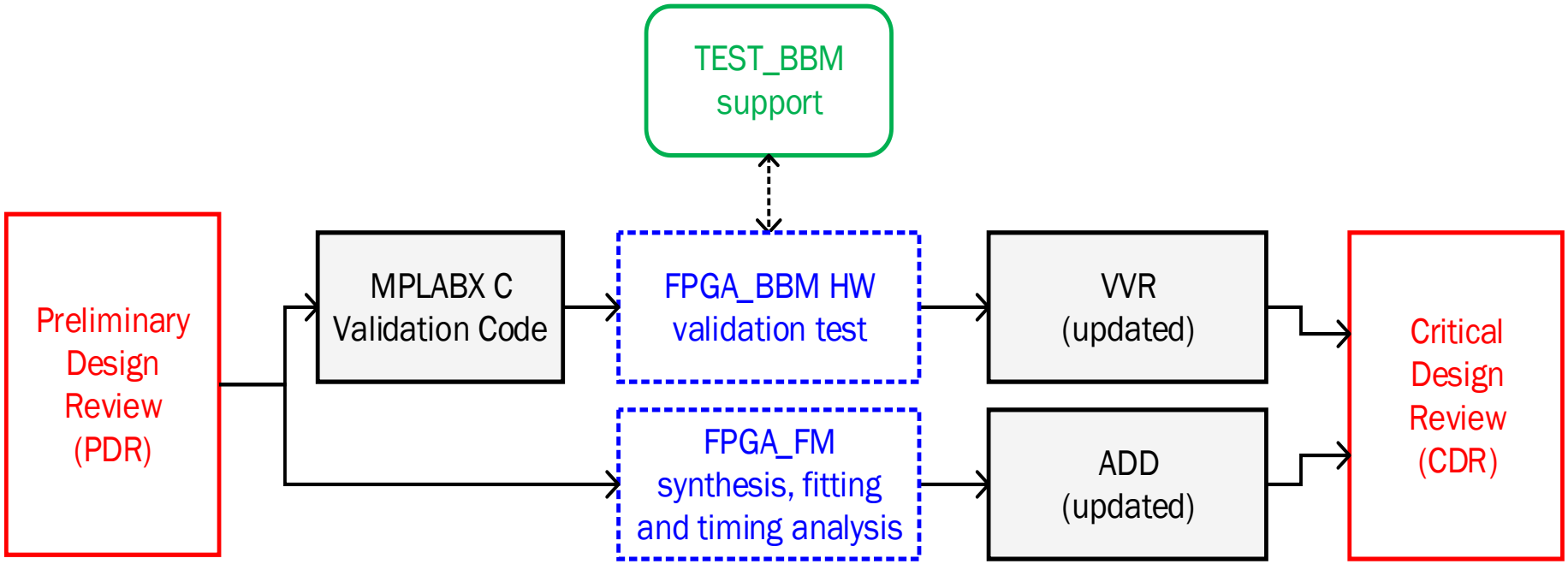
Architectural Design Phase

- HDL coding and RTL/Gate Level Simulations
- Production of the FPGA Detailed Design (ADD)
- Production of the FPGA Verification and Validation Plan (VVP)
- Design of the TEST_BBM

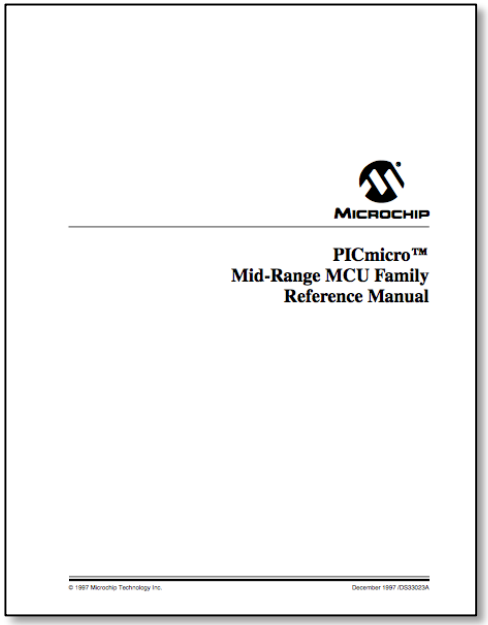


Detailed-Design Phase

- Synthesis, Fitting and Timing analysis on FPGA_FM
- HW Validation test using the FPGA_BBM and the TEST_BBM

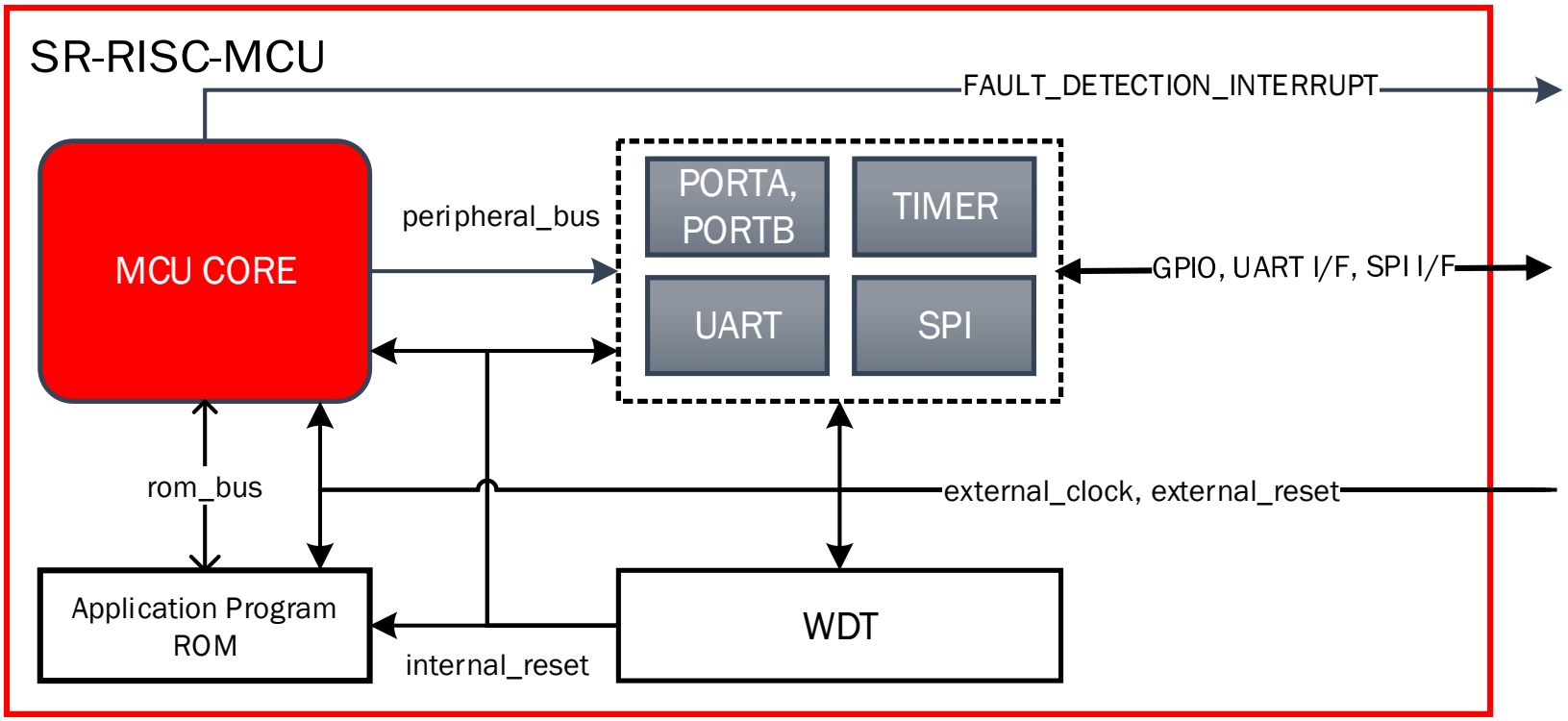


MCU core features

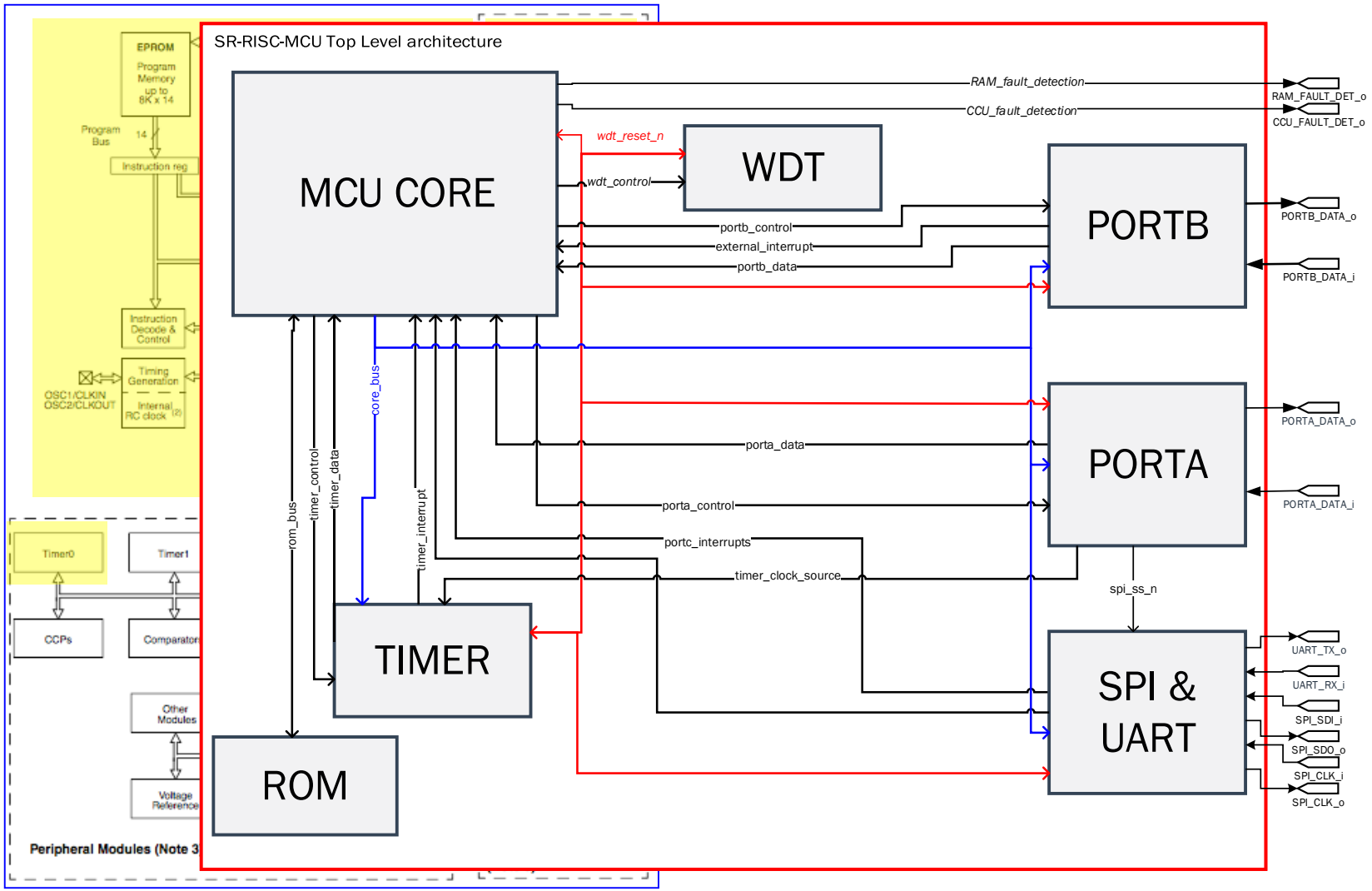


- 8-bit interruptible MCU Core
- Hard-coded monostable WDT
- 4 Peripheral interfaces
  - (2 GPIO, 1 UART, 1 SPI)
- 8-bit Timer with overflow detection
- 2 Fault-detection interrupts
- Fault injection capability (software based)
- Core SFRs physically separated from peripheral SFRs
- User RAM space parametrized between 192 and 368 bytes
- Compatible with PICmicro 16FXXX ISA
  - Using standard Microchip development tools in ASM and C

MCU core features (cont'd)



MCU core microarchitecture



MCU core radiation hardening

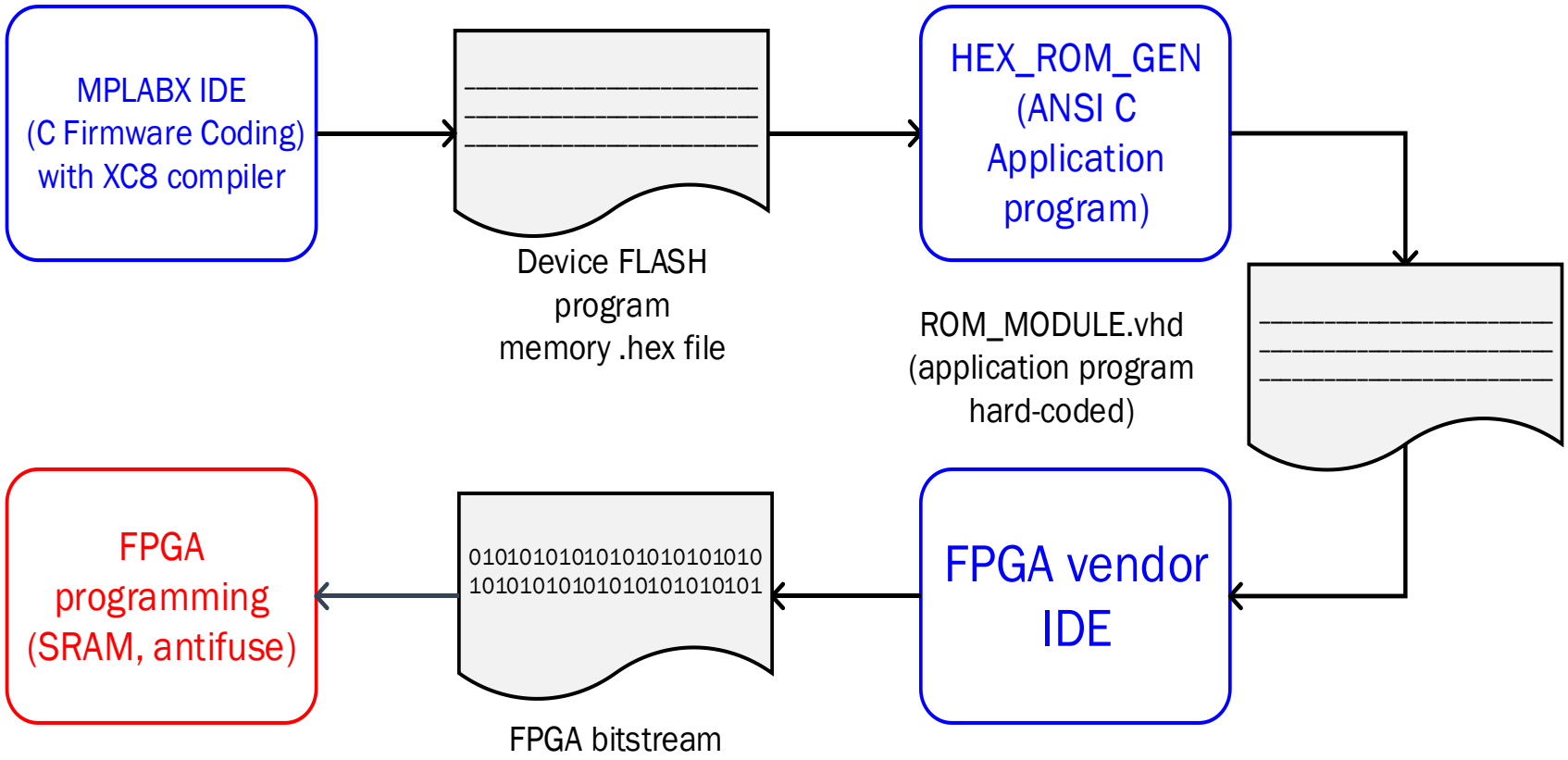
- Registers implemented with local-TMR
- Fail-safe finite state machines
- RAM protection with a custom implementation of SEC-DED EDAC coding (Hamming(8,4) + bit interleaving)
- Windowed Watchdog Timer reset period (1 s)
- Fault-error detection interrupt and external reset
- Possible (but not mandatory) implementation on MICROSEMI Antifuse-FPGA
  - SEU LET_{TH} greater than 37 MeV-cm2/mg
  - SEU memory upset rate less than 10E-10 errors/bit-day
  - SEL/SEGR immunity greater than 60 MeV-cm2/mg

FPGA implementation: synthesis and fitting results

- **FPGA_BBM** model based on ALTERA Cyclone IV SRAM-based
  - Total registers :1457 / 6,684 (21 %)
  - Combinational cells: 4017/ 6,272 (56%)
  - RAM cells : 3,072 of 276,480 (1 %)
  - Metastability Analysis (MTBF): 1e09 years
  - Timing Performance (WC) : 54 MHz

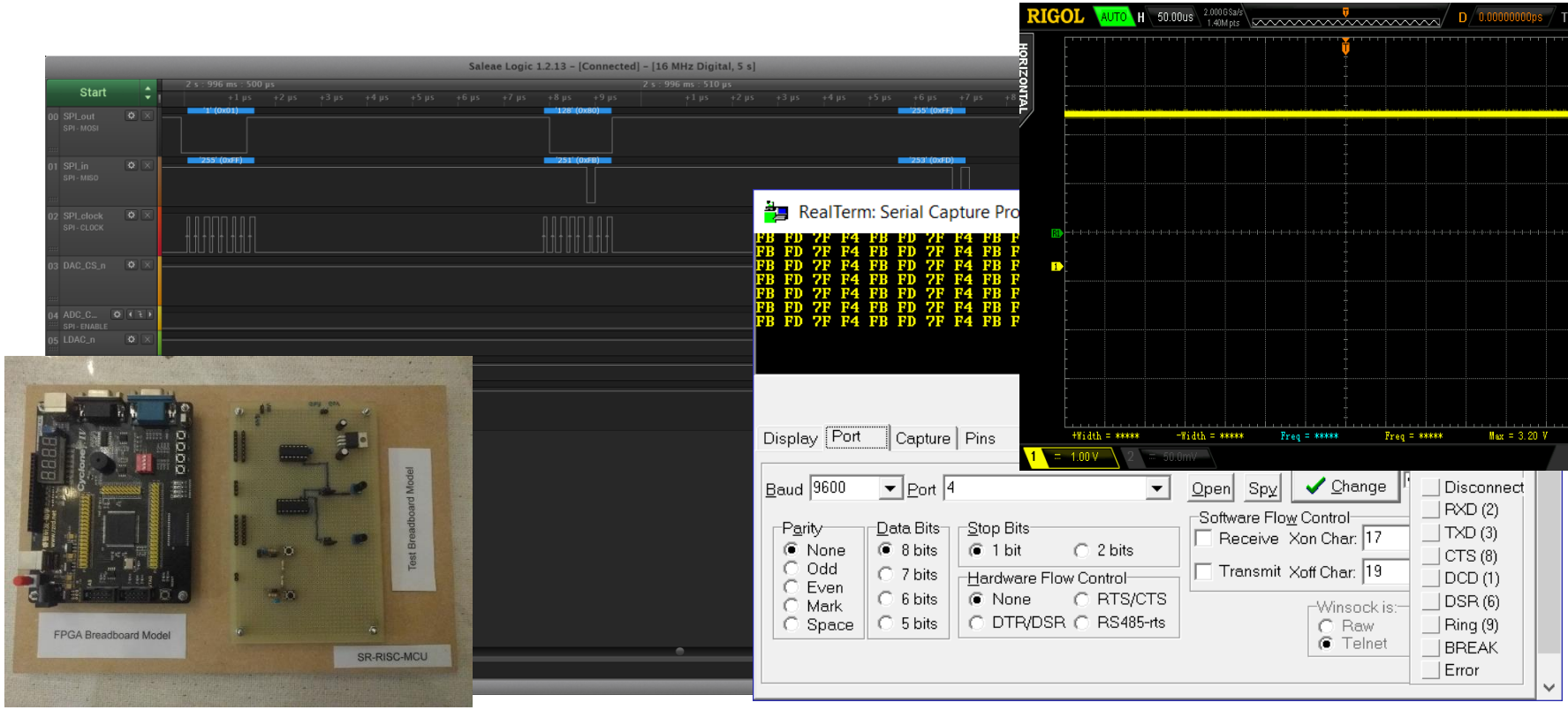
- **FPGA_FM** model based on MICROSEMI RTAXS-1000 Antifuse-based
  - Registers cells : 2506 of 12096 (21%)
  - Combinational cells: 747 of 6048 (12%)
  - RAM cells : 1 64k36 block (1 %)
  - TID estimated: 100 krad
  - Timing Performance (WC) : 43 MHz

IP core utilization toolchain



Hardware testing based validation

- **FPGA_BBM** model (RZ-EasyFPGA A2.1 devel. board)
- **TEST_BBM** model (custom breadboard based on MCP3008 A/D and MCP4912 D/A converters)



Conclusions…

- VHDL IP soft-core designed and verified in compliance to ESA/ECSS standard industrial cycle and related recommendations.
- Detailed hardware test based validation campaign
- Compatibility with industry-standard software development tools
- Availability of a VHDL microcontroller soft IP-core that can be used on-board in CubeSats for basic control and basic signal processing applications requiring high reliability and low cost

… and present/future perspectives

- Ground accelerated tests (using ENEA TOP IMPALART electrons/protons linear accelerator)
- Addition of new peripherals modules compatible with the original architecture (PWMs, I2Cs, SPI slaves, ecc..) and new ones (SpaceWire, AMBA/AXI, ecc…)
- Implementing and experimenting new radiation mitigation techniques (SW/HW)
- Software support for dealing with inaccurate data
- Porting the acquired now-how to the new emerging and open RISC-V instruction set architecture, for cross-platform redundancy

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Thank you for attention