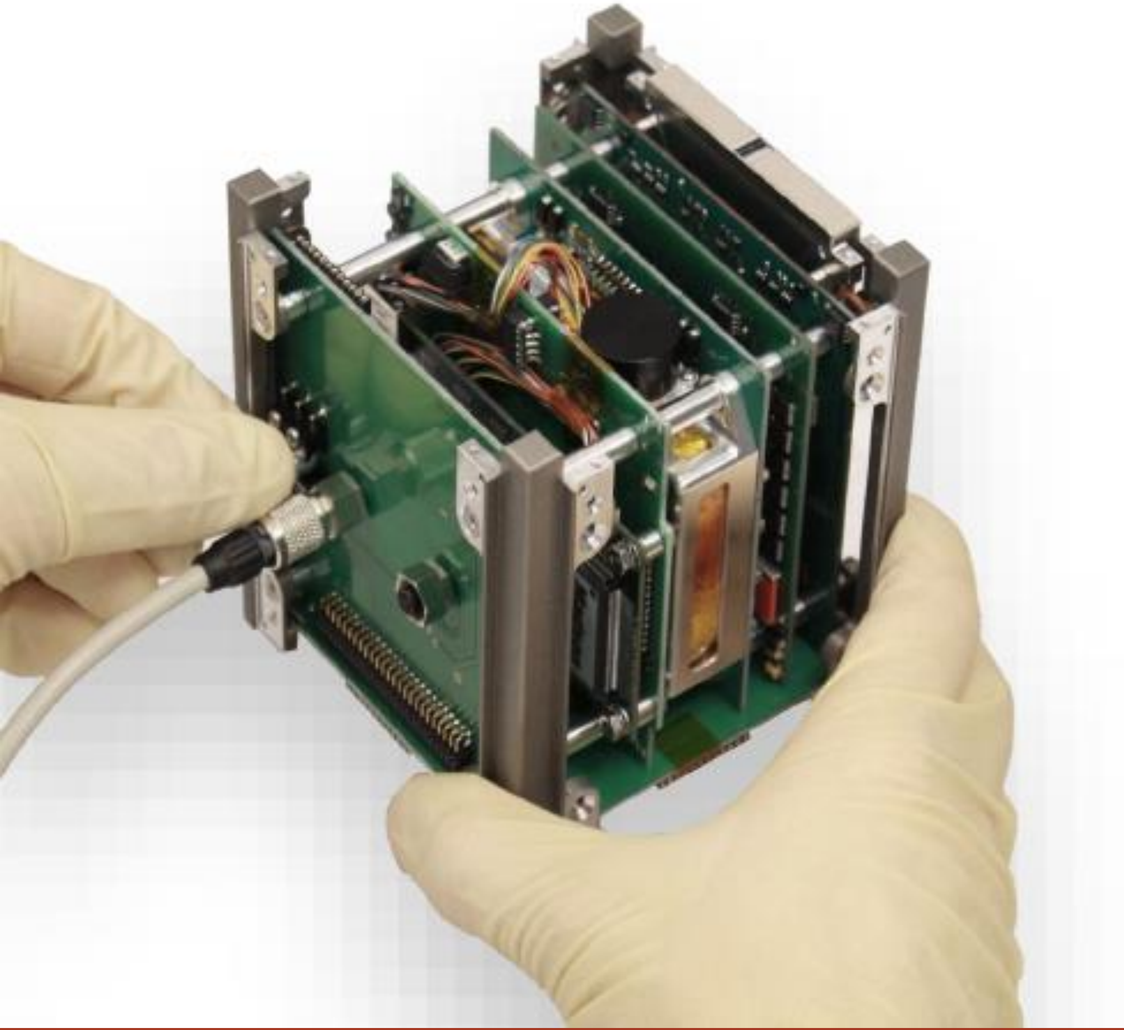
UNISEC Europe CSID – An Advanced Efficient Electrical Interface Standard for CubeSats

4th IAA Conference on University Satellite Missions and CubeSat Workshop

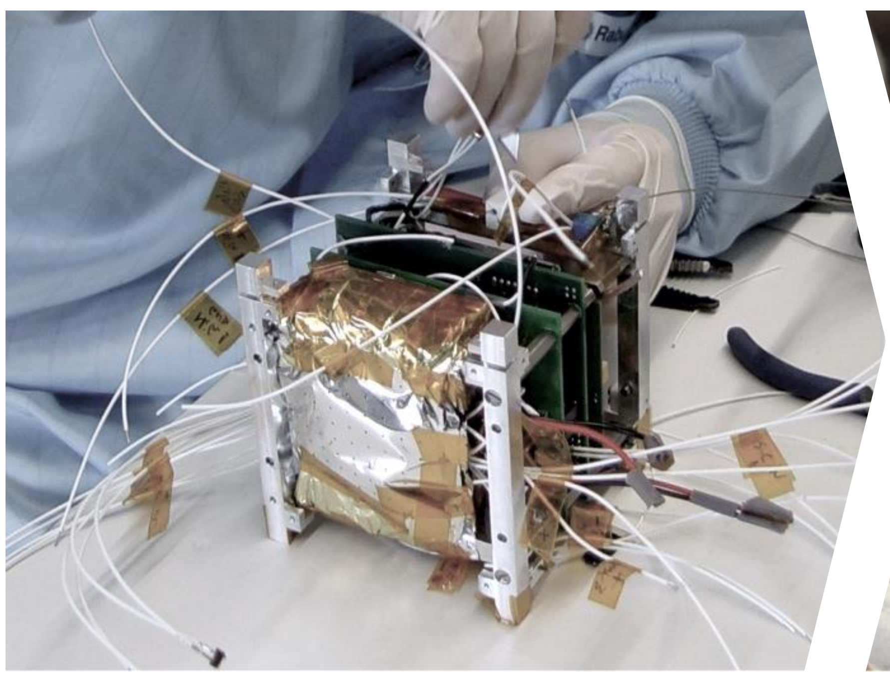


2017-12-07

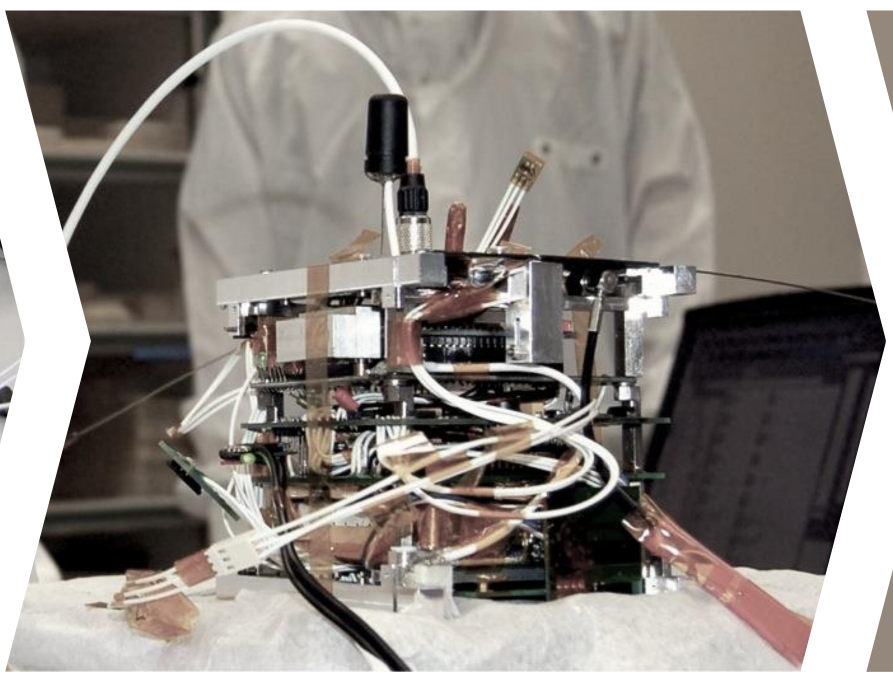
Oliver Ruf

Motivation

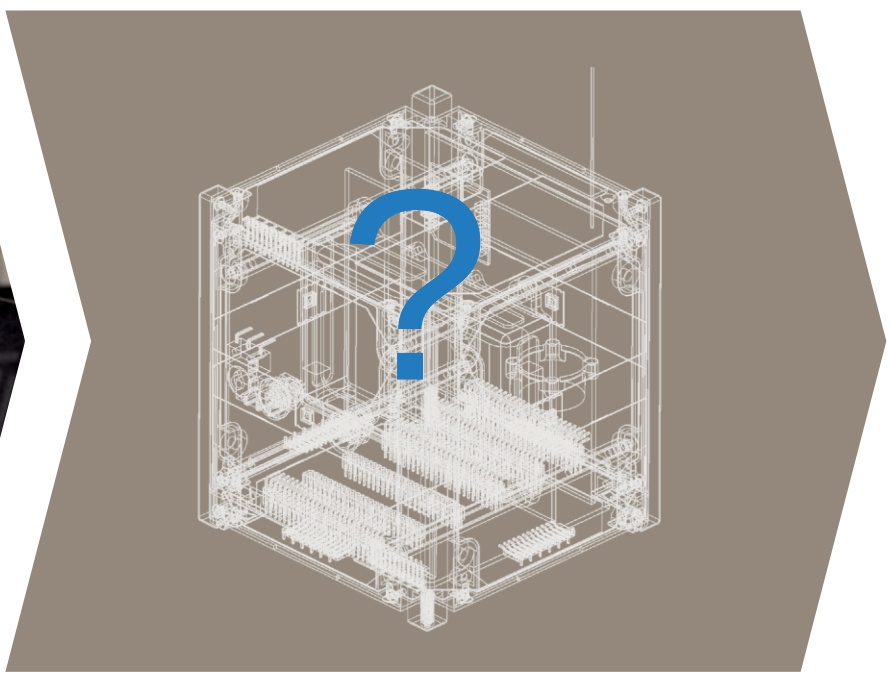
for a Standardization of Electrical Interfaces of CubeSats: Experience



- **UWE-1**



- **UWE-2**

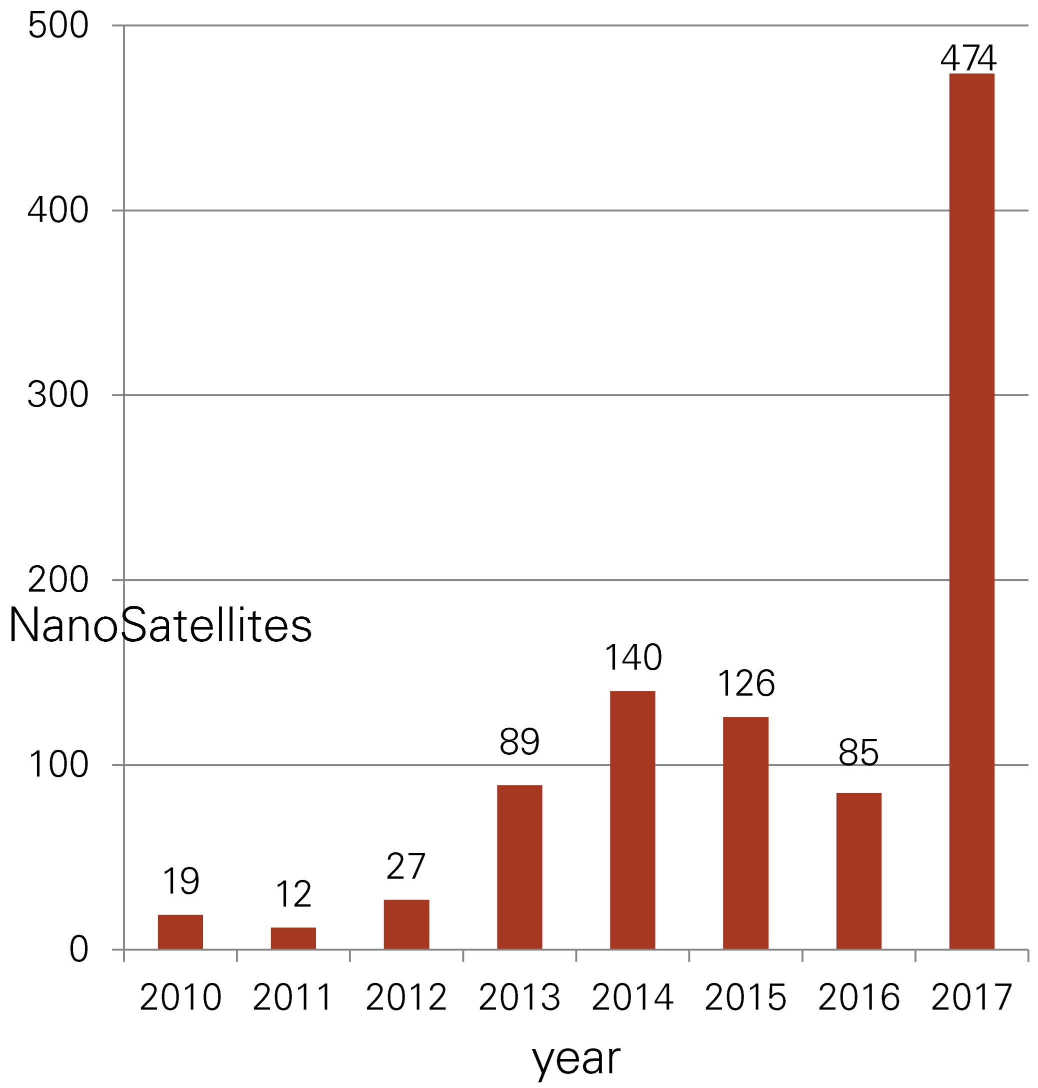


- **UWE-3**

Motivation

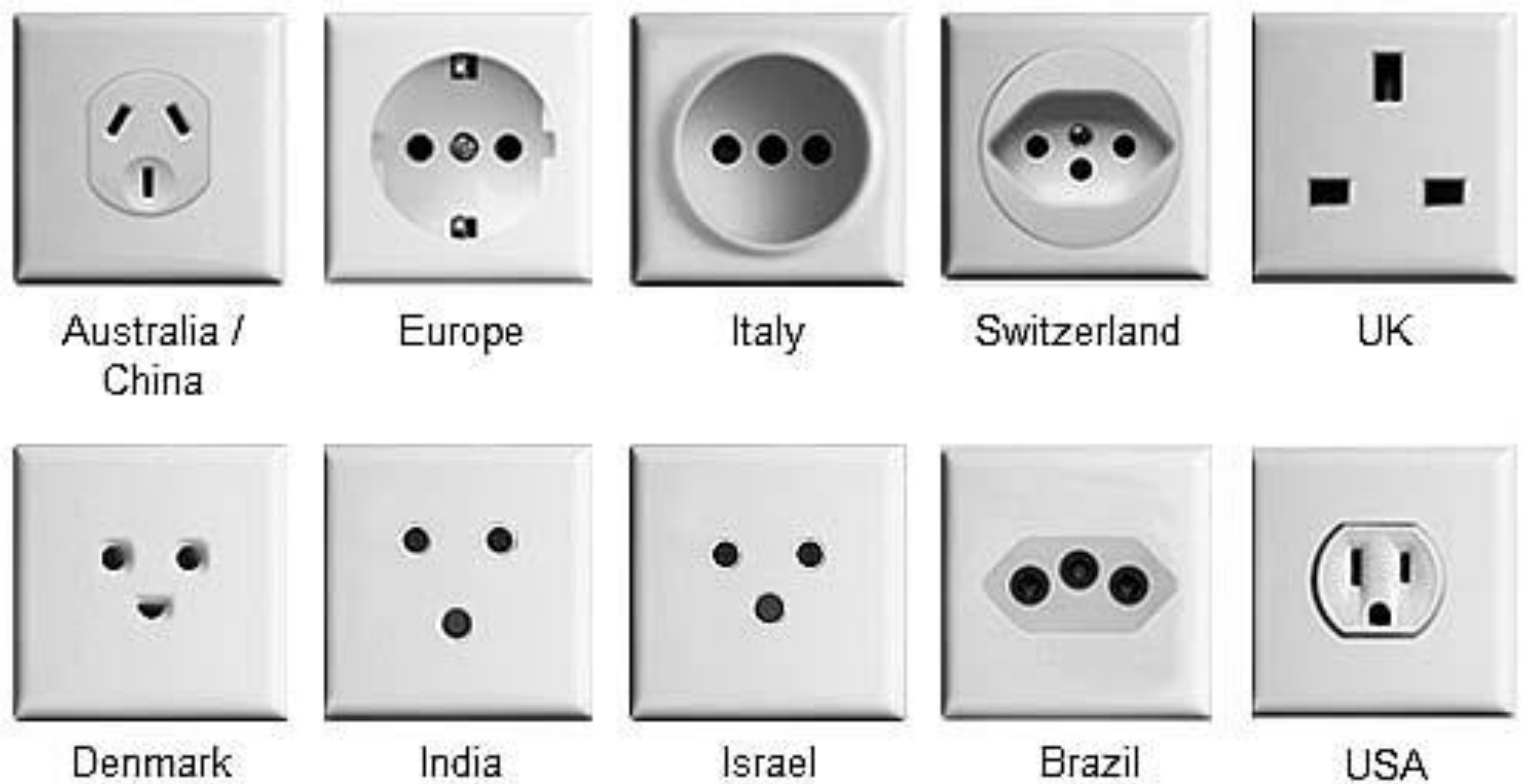
for a Standardization of Electrical Interfaces of CubeSats: Global market

- 474 scheduled and performed launches of NanoSatellites in 2017
- 1459 satellites operational end of 2016
- Key aspects
  - Performance: miniaturization is key driver to limit costs
  - Fast Development Cycle: design, iterate, and launch within a few months
  - Modern Production: production, integration & test: from high-tech manufactures to batch production



Motivation

for a Standardization of Electrical Interfaces of CubeSats: Global subsystem market



Motivation

for a Standardization of Electrical Interfaces of CubeSats: Durability & Reliability

40%

of all launched CubeSats failed to meet their mission goal

different studies show this is mostly due to

insufficient functional testing at system-level

Motivation

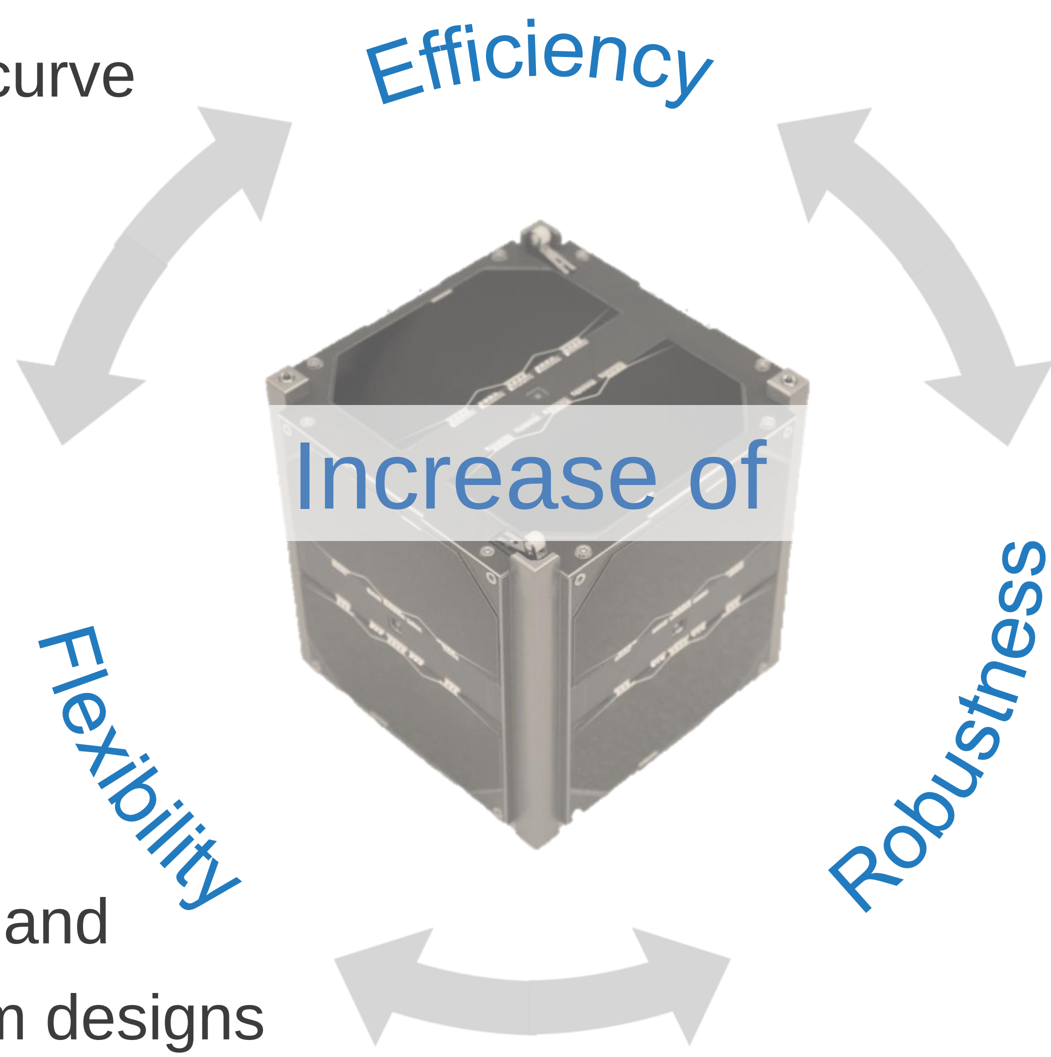
for a Standardization of Electrical Interfaces of CubeSats

- standardization is the key to economical utilization of small satellites in large numbers
- enables fast and reliable development, integration and verification
- standardized interfaces facilitate access to the system and increase testability and robustness

Chances

for a Standardization of Electrical Interfaces of CubeSats

- allow fast and compact integration
- simple maintenance of integrated bus
- support steep learning curve



- standardized monitoring and protection of subsystems
- standardized support for testing and debugging
- (in-orbit) re-programming of (integrated) subsystems

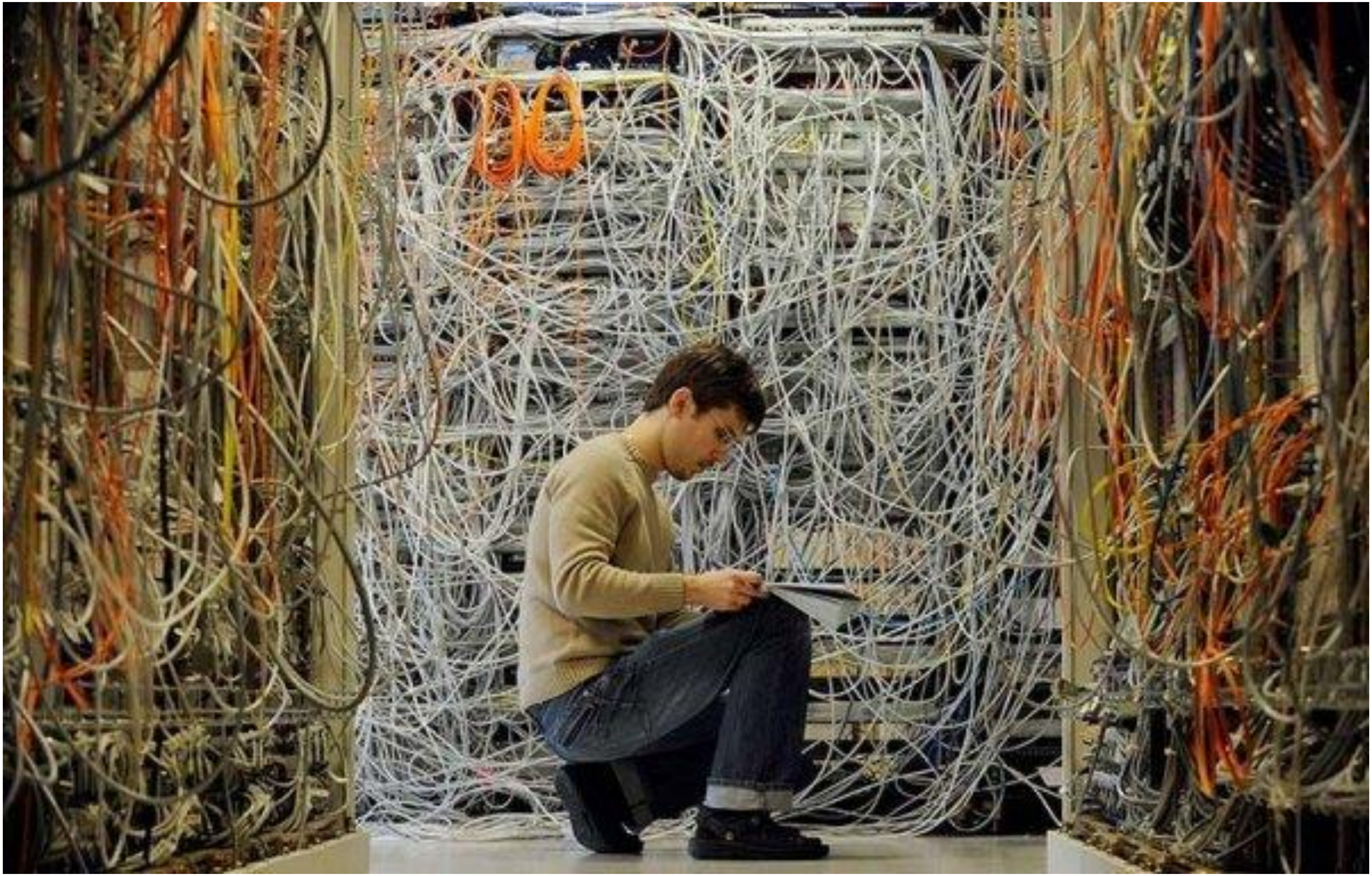
- support for scalability
- simplifies re-utilization and extension of subsystem designs

Limitations of current approaches

- PC/104:
  - 104 signals, many undefined and inconsistently used by different manufacturers, very large connector (20% of (inter-)board space)
  - all signals pass all connectors between source and sink
    → increased power loss and noise
- many important signals are currently not present on main connector
  → harnessing required for:
  - solar panel inputs
  - flight/kill switch logic
  - test, debug, programming interface for individual subsystems

		Cubesat Kit		GOM		Clyde	
		CubeSat Kit Motherboard Rev.E	CubeSat Kit Linear EPS Rev.D	NanoMind A712C	NanoPower P31u-9.0	Clyde CubeSat Power Distribution	Clyde 3G EPS
H1	1	GPIO		CANL		SW19	
	2	GPIO				SW19	
	3	GPIO		CANH		SW19	
	4	GPIO	CLK out			SW22	
	5	GPIO				SW23	
	6	GPIO				SW24	
	7	GPIO				A25	
	8	GPIO				A26	
	9	GPIO				A27	
	10	GPIO				A28	
	11	GPIO	ON_SD			A29	
	12	GPIO	GPIO			A30	
	13	GPIO					
	14	GPIO				A31	
	15	GPIO					
	16	GPIO				A32	
	17	RX1	RX1			A9	
	18	TX1	TX1			A33	
	19	RX0	RX0			A10	
	20	TX0	TX0			A34	
	21	SPI CLK	SPI CLK			A11	
	22	SPI MISO	SPI MISO			A35	
	23	SPI MOSI	SPI MOSI			A12	
	24	CS SDcard	CS SDcard			A36	
	25	OC FAULT	OC FAULT			A13	
	26	VREF0				A37	
	27	SENSE				A14	
	28	VREF2				A39	
	29	RESET	RESET			A15	
	30	VREF1				A40	
	31	OFF_VCC				A16	
	32	5V USB	5V USB		5V_in	A32	5V USB
	33	PWR MHX				A17	
	34	RST_MHX				RX	
	35	CTS_MHX				A18	
	36	RTS_MHX				TX	
	37	DSR_MHX				A19	SDA
	38	DXX_MHX				RX1	SCL
	39	TXD_MHX				A20	
	40	RXD_MHX				TX1	
	41	SDA	SDA	SDA	SDA	SDA	SDA
	42	VBACKUP 3V				RX2	GND
	43	SCL	SCL	SCL	SCL	SCL	SCL
	44	RSVDO reserved				TX2	
	45	RSVDO reserved				A21	
	46	RSVDO reserved				RX3	
	47			V PWM	PWR OUT1	A22	
	48			3.3V	PWR OUT2	TX3	
	49			V PWM	PWR OUT3	A23	
	50			3.3V	PWR OUT4	RX4	
	51			V PWM	PWR OUT5	A24	
	52			3.3V	PWR OUT6	TX4	

		Cubesat Kit		GOM		Clyde	
		CubeSat Kit Motherboard Rev.E	CubeSat Kit Linear EPS Rev.D	NanoMind A712C	NanoPower P31u-9.0	Clyde CubeSat Power Distribution	Clyde 3G EPS
H2	1	GPIO Ain				SW1	
	2	GPIO Ain				SW2	
	3	GPIO Ain				SW3	
	4	GPIO Ain				SW4	
	5	GPIO Ain				SW5	
	6	GPIO Ain				SW6	
	7	GPIO Ain				SW7	
	8	GPIO Ain				SW7	Switch1 12V or
	9	GPIO	ON USB			SW7	GND
	10	GPIO				SW8	Switch2 12V or
	11	GPIO				SW9	Switch3 12V or
	12	GPIO				SW10	Switch4 12V or
	13	GPIO				SW11	Switch5 5V
	14	GPIO				SW12	GND
	15	GPIO				SW13	Switch6 5V
	16	GPIO				SW14	Switch7 5V
	17	GPIO				SW14	GND
	18	GPIO				SW14	Switch8 3.3V
	19	GPIO				SW15	Switch9 3.3V
	20	GPIO				SW16	Switch10 3.3V
	21	GPIO				SW17	GND
	22	GPIO				SW18	GND
	23	GPIO				SW2ß	12V
	24	GPIO				SW21	12V
	25	5V	5V		5V	5V	5V
	26	5V	5V		5V	5V	5V
	27	VCC SYS	3.3V	3.3V	3.3V	3.3V	3.3V
	28	VCC SYS	3.3V	3.3V	3.3V	3.3V	3.3V
	29	DGND	GND	GND	GND	GND	GND
	30	DGND	GND	GND	GND	GND	GND
	31	AGND	AGND		AGND	AGND	AGND
	32	DGND	GND		GND	GND	GND
	33	S0	S0				
	34	S0	S0				
	35	S1	S1				PCM in
	36	S1	S1				PCM in
	37	S2					RBF SW
	38	S2					RBF SW
	39	S3					SEP SW1
	40	S3					SEP SW2
	41	S4	S4				BCR OUT
	42	S4	S4				BCR OUT
	43	S5	S5				BCR OUT
	44	S5	S5				BCR OUT
	45	VBATT 7-10V	VBATT 7-10V		V_BAT	Battery	BAT
	46	VBATT 7-10V	VBATT 7-10V		V_BAT	Battery	BAT
	47					RS422 RX A	GND
	48					RS422 TX A	GND
	49					RS422 RX B	
	50					RS422 TX B	
	51					optional V	
	52					optional V	



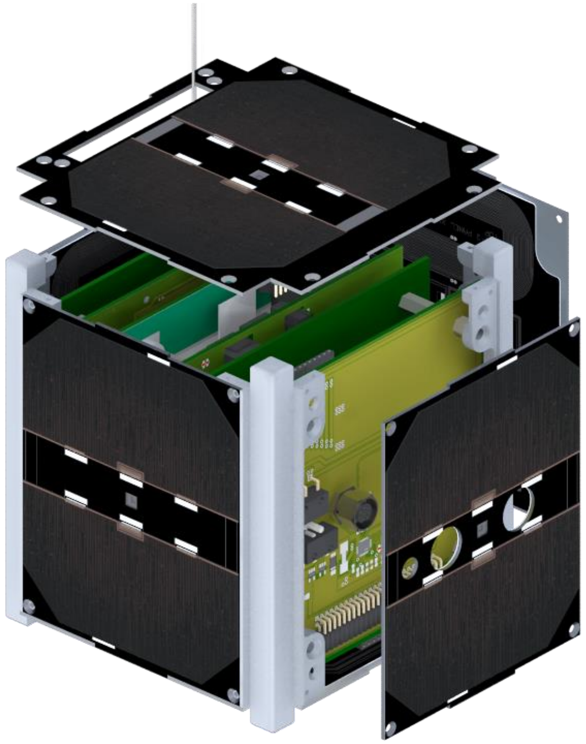
Limitations of current approaches

- often missing signals
  - e.g. sync signal for time/clock synchronization between subsystems
- Lack support for redundancy concepts
  - separate unregulated battery power paths
  - redundant data communication buses, concept for redundancy selection
  - dedicated communication buses for crucial subsystem control (e.g. OBC-COMM, OBC-EPS)

UNISEC Europe Bus

Generalized Debug & Maintenance Interface

- modular architecture based on backplane
- debug support for ANY microcontrollers on ALL subsystems (via OBC)
- full access to each subsystem via umbilical even when satellite is completely / tightly integrated
- external debug interface (extra standardized interface for stand-alone operation) provided by USB-Interface

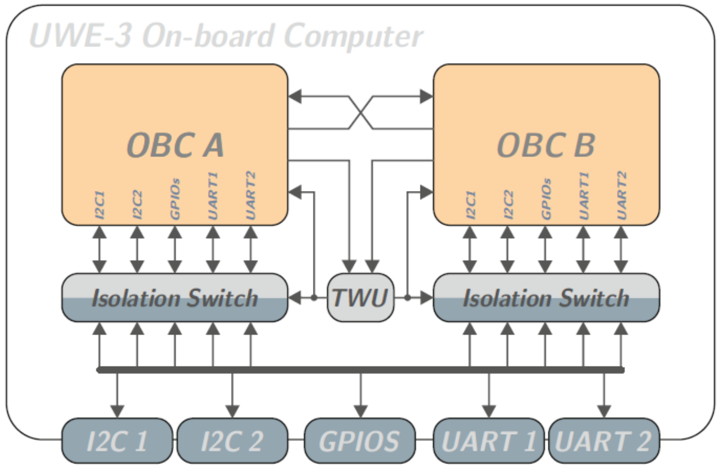


UNISEC Europe Bus

Digital Communication

- dedicated signal lines for control of most crucial standard subsystems, e.g.:
  - OBC-COMM: dedicated serial communication lines for redundant communication subsystem
  - OBC-EPS: dedicated control lines for redundant power paths
- redundant data communication buses, e.g.:
  - 2x I2C: standard low rate / low power consumption communication for subsystem control and housekeeping

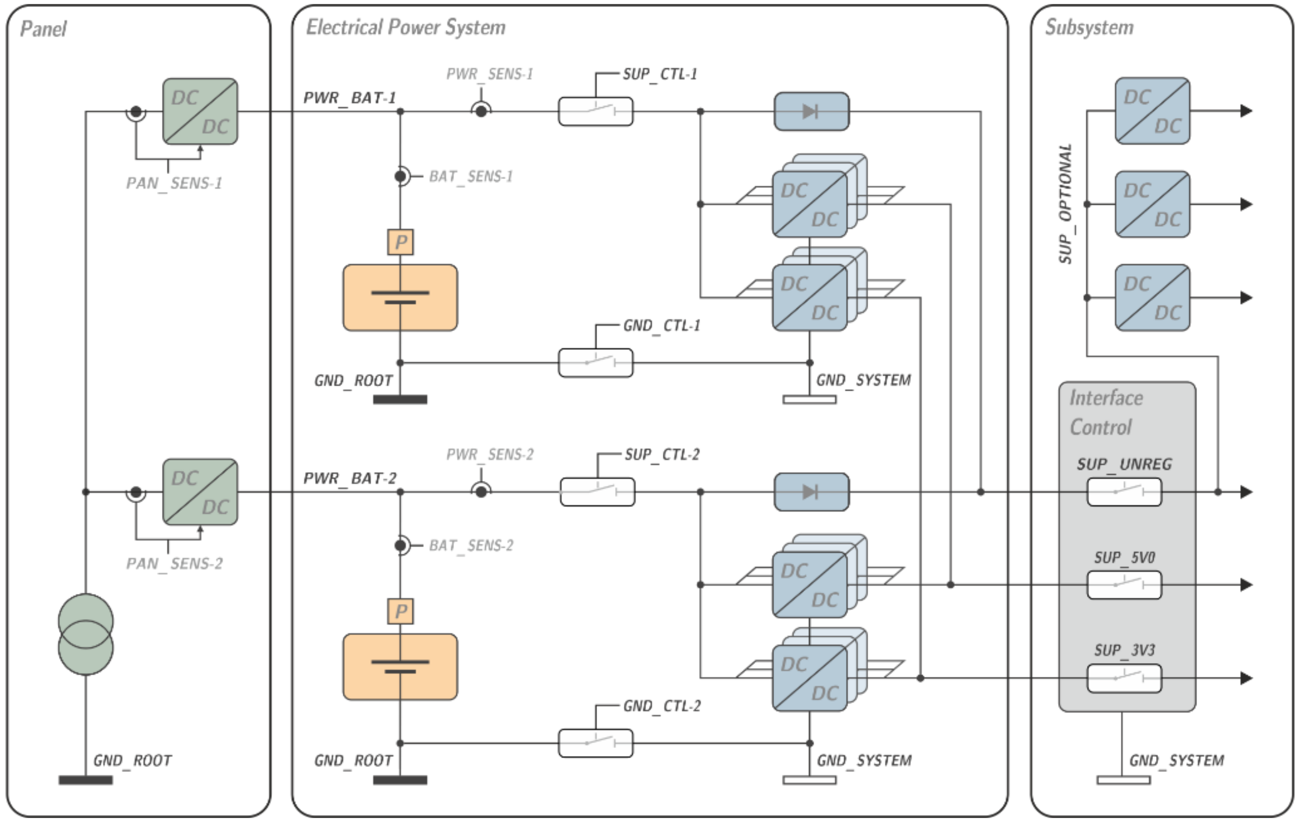
    and
  - 2x M-LVDS (full duplex: 8 pins) for high rate / high power consumption communication for payload data bus, high speed downlink from data pool
- time synchronization between subsystems (pulse per second)



UNISEC Europe Bus

Modular Distributed Electrical Power System

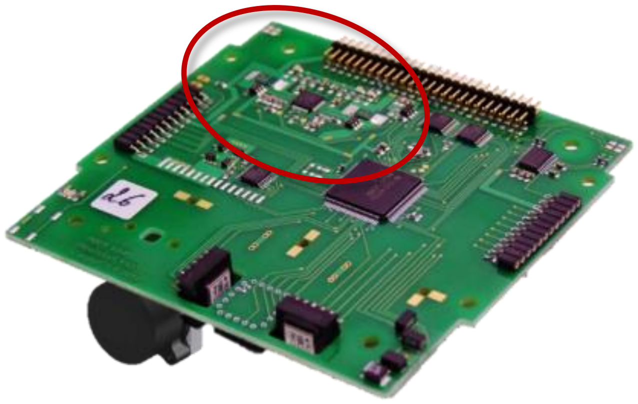
- Distributed Power Generation
  - MPPT circuitry can be part of “more intelligent” solar panels
  - can directly supply (redundant) unregulated power bus
    - Minimal impact on required signals on satellite bus
    - Power System capabilities scale with connected power generators
    - Optimal design of MPPT circuitry w.r.t. solar panel
    - Supports arbitrary number of panels with heterogeneous performance

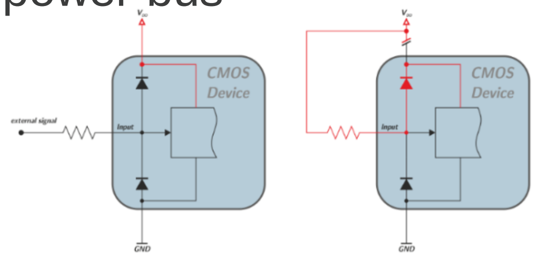


UNISEC Europe Bus

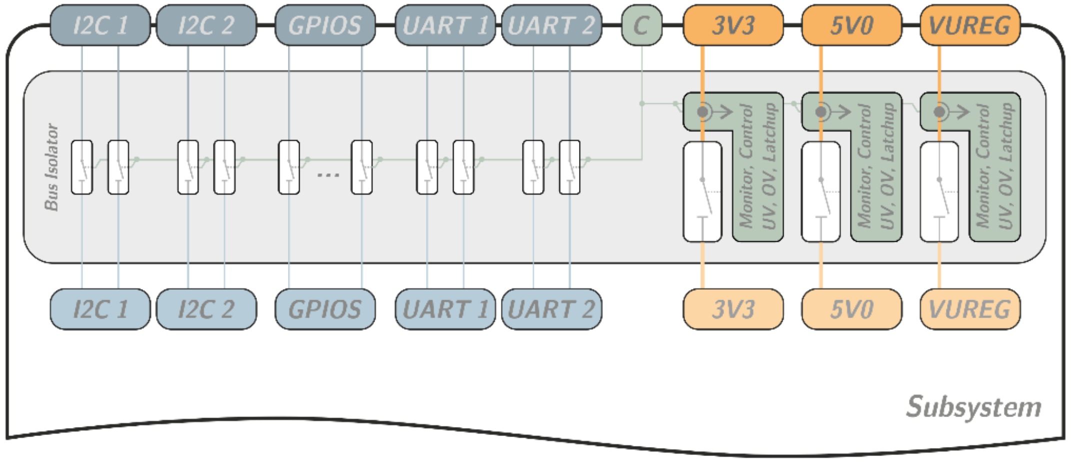
Modular Distributed Electrical Power System

- Distributed Power Distribution
  - standardized subsystem interface control circuitry included on ALL subsystems
  - power switch, monitoring, protection (OV, UV, OC)
    - optimized for actual subsystem
    - minimizes impact on required signals on satellite bus (no dedicated switched power line for each potential subsystem)
  - selective isolation of data interface from satellite bus
    - required for proper partial power down, avoids current leakage for switched off subsystems
    - can also handle data bus or power bus redundancy selection in a standardized way





undesired current leakage via data interface of powered down CMOS device



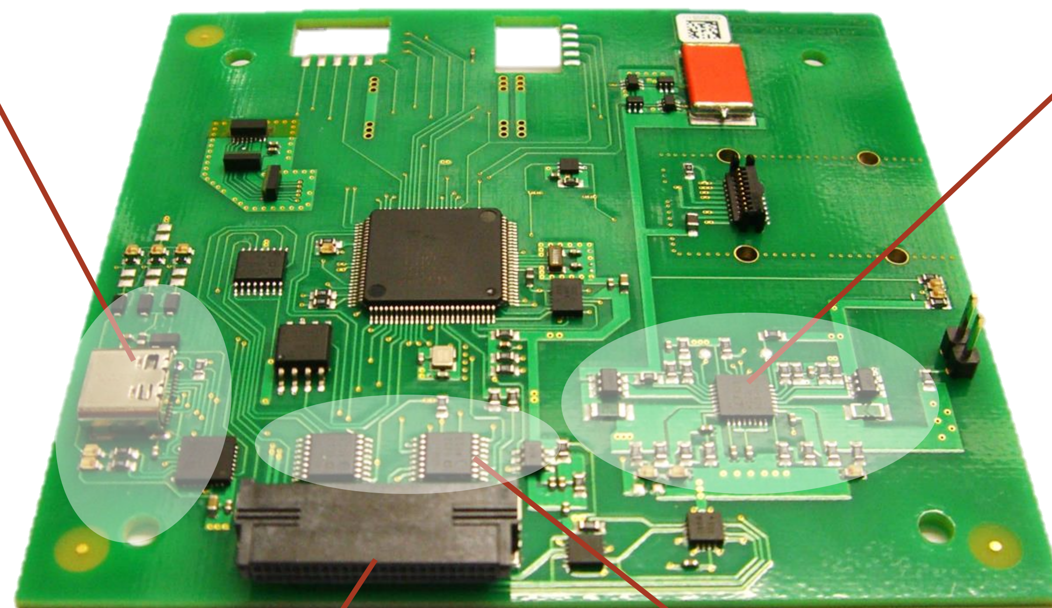
UNISEC Europe Standard Interface Control Circuit

UNISEC Europe Bus

CubeSat Subsystem Interface Definition

External Debug Interface

- easy stand-alone operation of subsystem
- debug communication (UART via USB bridge)
- microcontroller programming and in-system-debugging (JTAG, SBW, SWD)
- supply by USB power (5V, 3.3V, unregulated bus)



Power Control Circuit

- controlled by OBC via redundant I^2C bus
- power switch
- power monitoring (voltage, current)
- power protection optimized for specific subsystem (over-voltage, under-voltage, over-current, i.e. latchup)

Satellite Bus Connector

- compact and robust backplane
- redundant power, high-speed and low-speed digital buses
- dedicated signals for reset, time sync, deployment logic
- internal debug interface (communication, programming, and debugging after integration and in-orbit)

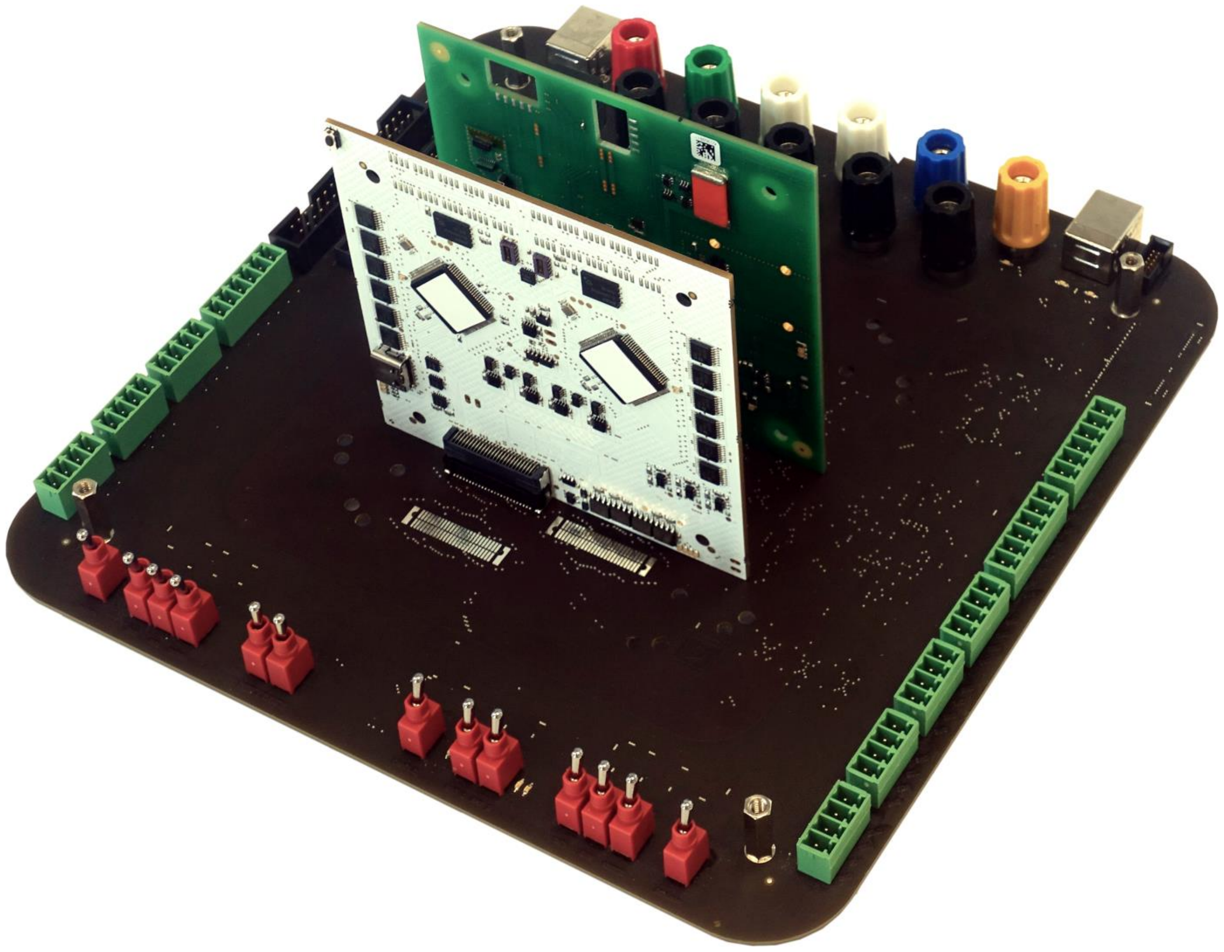
Interface Control Circuit

- selective bus isolation
- prevents current leakage for partial power down
- allows bus routing, redundancy selection controlled by OBC

UNISEC Europe Bus

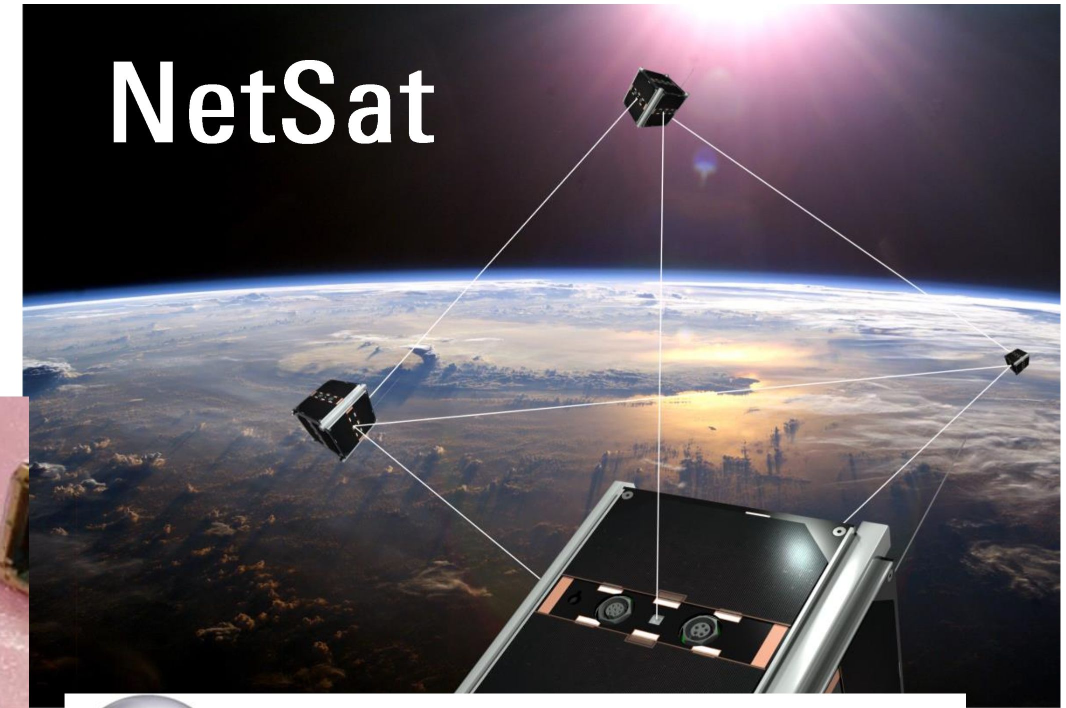
Satellite Development Board

- supports flexible and efficient satellite development
- allows rapid system assembly for efficient functional integration testing
- provides comfortable access to all relevant interfaces on the bus for efficient measuring and testing
- integrates UNISEC umbilical line specification providing a USB interface and various programmer interfaces
- simulates OBC or subsystems by integrated powerful MCU



UNISEC Europe Bus

Implementations & Missions



Conclusions

- Small Connector enables very tight integration

  →decreases launch cost drastically

- Increases flexibility, efficiency and robustness

  →Prevents you from errors and enables rapid & reliable development, integration and testing, interchangeability, …

- # Open Source

  →download specifications: http://unisec-europe.eu/standards/bus/

PS: Back to UWE-3

- Integration and final testing took only 2 hours
- Fully operational since 21st Nov. 2013

→ today **1489** days

HAPPY BELATED BIRTHDAY UWE-3