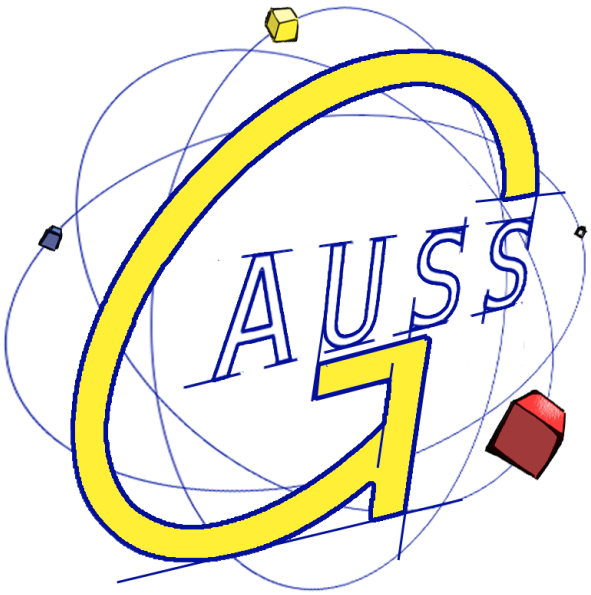
GAUSS: ABACUS 2017

User Selectable Options Sheet

[ABACUS2017_201703]



Group of Astrodynamics for the Use of Space Systems

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Acronyms

OBC	On Board Computer
PCB	Printed Circuit Board
FPGA	Field Programmable Gate Array core
MCU	Microcontroller Unit
SDA	Serial Data Line in I2C Bus
SCK	Serial Clock Line in I2C Bus
GPIO	General Purposes Input Output
LVDS	Low Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter-Coupled Logic
PLL	Phase-Locked Loop
IMU	Inertial Measurement Unit
DoF	Degrees of Freedom
IRQ	Interrupt Request

1. Introduction

ABACUS 2017 is the fourth revision of the ABACUS OBC series designed and build in Italy by the company GAUSS Srl. ABACUS features a MSP430 MCU and a Spartan 3E FPGA. ABACUS has flown already on several missions (UniSat-5, UniSat-6, Unicubesat-GG, Tigrisat and Serpens). The core components of the board have not changed during the different revisions of the board.

ABACUS has some hardware flexibility in order to render the OBC as much compatible as possible with other components of your satellite. The user has to decide during the final production phase of the board some of these options. The selections chosen will be hardwired on the PCB. Under the sole responsibility of the customer, every selection can be modified in the future by the final user. Some of these possible options are also graphically reported on the PCB.

ABACUS 2017 has some pinout differences with previous revisions of the board but for legacy reasons the user can decide to apply some user selectable configurations that renders ABACUS 2017 identical to ABACUS 2014 from the pinout perspective.

2. Blocks Diagram, Connectors and Pinout overview

For updated information on available connections, pinouts and detailed description on the board, please refer to the document “ABACUS Datasheet” available online at https://www.gaussteam.com/services/satellite-subsystem/onboard-computer/abacus-2/

3. Options Sheet Selection Guide

On this section a full description of the User Selectable Options sheet is given. Each modification of the board not executed by the GAUSS Team will be at responsibility and own risk of the customer.

3.1. GPIO Expander

The MCU (MSP430 EP Series) is connected via I2C to a GPIO Expander with its 16 GPIOs connected to the PC/104 connector (H1 and H2). The I2C bus used by the GPIO Expander and the MCU is physically the same used by many satellites on pin H1_41 (SDA) and H1_43 (SCK) of the PC/104 connector, for this reason, to avoid conflicts with other systems on the PC/104 connector, on ABACUS 2017 there are two options for the I2C address of the GPIO Expander.

Address I2C - 0x020	R73 = 0Ω, R72 = empty
Address I2C - 0x021	R72 = 0Ω, R73 = empty

Moreover, for compatibility with other boards with different voltage levels, the 16 GPIO ports can be powered from the internal voltage (3.3V) or from an external voltage (from 1.8V to 5V) on the pin H2_17.

Internal 3.3V	R74 = 0Ω, R75 = empty
External Voltage (1.8V up to 5V)	R75 = 0Ω, R74 = empty

Note: At least one of the two addresses of the GPIO Expander, have to be left unused from any other subsystems using the I2C Bus on pin H1_41 (SDA) and H1_43 (SCK) of the PC/104 connector.

3.2. UART1_TXD / GPIO

For compatibility with other sub-systems, it is possible to leave both of H1_3 or H1_2 pins on PC/104 connector unconnected. The signal involved in that change is the transmission line of the UART1 port, also usable as GPIO pin (MCU pin P5.6).

UART1_TXD connected to H1_3	R18 = 0Ω, R17 = empty
UART1_TXD connected to H1_2	R17 = 0Ω, R18 = empty
Not Used	R18 and R17 empty

Note:

- ABACUS 2017 would be equivalent to ABACUS 2014 if UART1_TXD/GPIO is connected to H1_3;
- the H1_3 is often used by other sub-systems as part of the CAN bus;
- Keep in mind that in ABACUS 2014, H1_2 is used as GND.

3.3. I2C Pull-Up resistors

On the PC/104 connector the I2C 3.3V Bus is connected to the pins H1_41 (SDA) and H1_43 (SCK) that is generally the I2C bus of the satellite. ABACUS by default has the two Pull-Up resistors of the I2C bus connected to 3.3V. However, if other subsystem already have the I2C resistors connected the user might desire to not install them.

PullUp Resistor	R13
PullUp Resistor	R14

3.4. ADC11/GPIO

On the PC/104 connector there are several ADC/GPIO channels. The signal ADC11/GPIO (MCU pin P7.7) can be used as ADC/GPIO channel on the pin H1_25 of the PC/104 connector or it can be used, as ADC input, to monitor the pin FPGA DONE signal of the FPGA core. The FPGA DONE signal goes high (high = in the range of 0.7V to 2.5V) when the FPGA is correctly programmed. The user can monitor if the FPGA has been correctly programmed visually with a LED already installed on the board and also with the MCU using the ADC11 input.

The user must decide if use the ADC11 to monitor the FPGA or to connect it on the H1_25. Not connecting any of the resistors leaves the H1_25 unconnected for other purposes.

MCU Connected to the FPGA DONE signal	R88 = 0Ω, R89 = empty
MCU Connected to H1_25	R89 = 0Ω, R88 = empty
Not Used	R88 and R89 empty

Note: Abacus 2017 is equivalent with Abacus 2014 if ADC11/GPIO is connected on H1_25.

3.5. RTC IRQ output

The I2C Real Time Clock present on the board has an IRQ pin (with a PullUp resistor to 3.3V) that can be connected to the FPGA pin 178 or to the MCU pin P2.0 and to the pin H1_8 on the PC/104 connector. Connecting the IRQ to the MCU means that it would be connected also to the pin H1_8. This RTC IRQ output can be used as a 1Hz or 512Hz output for other subsystems.

Connected to MCU pin P2.0 and H1_8	R76 = 0Ω, R77 = empty
Connected to FPGA pin 178	R77 = 0Ω, R76 = empty
IRQ Not Used	R76 and R77 empty

3.6. FPGA VCCO_1 Power Source

The signals of the Bank_1 of the FPGA are all connected as general purpose user pins on the connector P7. Based on the use of those pins (for example as GPIO or LVDS signals) the user can chose its voltage that is done modifying the voltage of the power pins VCCO_1. By default VCCO_1 is connected to 3.3V so the P7 pins are 3.3V.

Internal 1.2V	R82 = 0Ω, R81 and R83 = empty
Internal 2.5V	R81 = 0Ω, R82 and R83 = empty
Internal 3.3V	R83 = 0Ω, R81 and R82 = empty

Note: to use the P7 signals as LVDS or LVPECL, VCCO_1 power source has to be 2.5V. The FPGA only supports the voltage range of the standard LVDS_25 or LVPECL_25 as low voltage differential signaling standard.

3.7. FPGA Clock

A PLL and a Crystal of 25MHz are the source of the clock for the FPGA. The PLL can be set as x1 or x4 multiplier so the clock of the FPGA can be 25MHz or 100MHz. Keep in mind that increasing the clock speed means not only increased performance but also increased power consumption.

25MHz	R55 = 5.1KΩ, R54 = empty
100MHz	R54 = 5.1KΩ, R55 = empty

Note: the selection resistor has to be 5.1KOhm

3.8. IMU IRQ output

The 9-DoF IMU has an IRQ output pin (with a PullUp resistor to 3.3V) that can be connected to the MCU pin P2.3 or to the FPGA pin 200 but also it can be left unused.

Connected to MCU pin P2.3	R63 = 0Ω, R80 = empty
Connected to FPGA pin 200	R80 = 0Ω, R63 = empty
IRQ Not Used	R63 and R80 empty

3.9. RS422/485 adapter

On ABACUS you have the possibility of using the UART0 signals of the MCU as RS422/485 differential signals. These differential signals can be used in Full Duplex mode (4 wires, 2 differential pairs) or in Half Duplex mode (2 wires, 1 differential pairs). These options are programmatically selected by the MCU, however the user has to decide whether or not to install the termination resistors based on its satellite connections.

Full Duplex mode	R87=RX termination, R84=TX termination, R85 and R86 = empty
Half Duplex mode	R85 and R86 = 0Ω; R84 or R87 = termination resistor

User Selectable Options Sheet

ABACUS 2017

Mark the corresponding white square for the desired options. Refer to the ABACUS 2017 – Options Sheet Selection Guide. In case of no mark it will be considered the default option.

Note: NC = not electrically connected on the board, pins are free to be used for other sub-systems.

GPIO Expander I2C Address:

☐	Address I2C - 0x020 (**Default**)	
☐	Address I2C - 0x021	

GPIO Expander Power Source:

☐	Internal 3.3V (**Default**)	In this case H2_17 is NC
☐	External Voltage (1.8V up to 5V)	The input pin of the external voltage is H2_17

UART1_TXD / GPIO:

☐	Connected to H1_3	Abacus 2014 legacy. Conflict with CAN bus of some CubeSat boards. In this case H1_2 is NC
☐	Connected to H1_2 (**Default**)	Abacus 2014 GND conflict. In this case H1_3 is NC
☐	Not Used	In this case H1_2 and H1_3 are NC and MCU pin P5.6 is not used

I2C Bus Pull-Up to 3.3V resistors:

☐	3.3 KOhm resistors (**Default**)	
☐	1.5 KOhm resistor	
☐	None	

ADC11 / GPIO:

☐	Connected to H1_25	Abacus 2014 legacy
☐	Connected to the FPGA DONE signal (**Default**)	In this case H1_25 is NC
☐	Not Used	In this case H1_25 is NC and MCU pin P7.7 is not used

RTC IRQ output:

☐	Connected to MCU pin P2.0 and H1_8	FPGA pin 178 is not used
☐	Connected to FPGA pin 178	In this case H1_8 is connected to MCU pin P2.0
☐	IRQ Not Used (**Default**)	In this case H1_8 is connected to MCU pin P2.0

FPGA VCCO_1 Power Source (BANK_1 on P7 connector):

☐	Internal 1.2V	
☐	Internal 2.5V	Mandatory using LVDS connection
☐	Internal 3.3V (**Default**)	

FPGA Clock:

☐	25 MHz	On board PLL x1 from a 25MHz crystal
☐	100 MHz (**Default**)	On board PLL x4 from a 25MHz crystal

IMU IRQ output:

☐	Connected to MCU pin P2.3	In this case FPGA pin 200 is not used
☐	Connected to FPGA pin 200	In this case MCU pin P2.3 is not used
☐	IRQ Not Used (**Default**)	In this case FPGA pin 200 and MCU pin P2.3 are not used.

RS422/485 configuration (adapter for UART0):

☐	Full Duplex 4 wires connection (**Default**):		
	☐ R-Terminations not installed (**Default**)	☐ R-Termination 120 Ohm on receiver	☐ R-Terminations 120 Ohm on transmitter and receiver
☐	Half Duplex 2 wires connection:		
	☐ R-Termination not installed	☐ R-Termination 120 Ohm	

Launch Date (optional):_____ Satellite/Payload Name (optional):_____

Customer/Responsible: Name:_____Surname:_____

Date _____,

Confirmation Signature of the Customer / Responsible: _____